NOVEL III-V MOSFET INTEGRATED WITH HIGH-K DIELECTRIC AND METAL GATE FOR FUTURE CMOS TECHNOLOGY

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NATIONAL UNIVERSITY OF SINGAPORE

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Summary

This project has developed the process to fabricate novel III-V MOSFET. The main process steps include pre-gate cleaning, CVD high-k gate dielectric deposition, gate electrode deposition and etching, selective source and drain implantation, dopant activation and contact formation.

The Silicon implantation is used to form n^+ source and drain. Contact resistance, sheet resistance and junction characteristic are studied. RTA temperature and time are calibrated. It is found that InGaAs enables a relatively low temperature for activation.

The CVD HfAlO and HfO_2 gate dielectrics are directly deposited onto the InGaAs after pre-gate cleaning. It is found that InGaAs, with high Indium concentration, has better integration compared to GaAs. With sputtered TaN metal gate electrode, the MOS capacitor is studied. The MOSFET is then fabricated by an implanted source and drain selectively self-aligned to the gate.

Next, interface engineering with the plasma PH_3 passivation is introduced to the MOSFET fabrication. Detail analysis by XPS shows the chemical composition on the surface after PH_3 treatment. Passivation results in the improvement of surface quality and helps in the InGaAs integration with high-k dielectric. Transistor performance has a significant enhancement. Two important figures of merit, on-state current and subthreshold swing, are compared with the directly deposited control devices. Electron mobility is extracted by a split C-V method.

With the advantage of self-alignment, scaling of the MOSFET becomes much easier. The short channel InGaAs MOSFET is fabricated by a novel approach. The gate is patterned by Electron Beam Lithography and Platinum hard mask. It is

demonstrated that 40 nm gate line can be achieved by this method, and high performance for small channel length MOSFET is reported.

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List of Abbreviations

ALD	Atomic Layer Deposition
AZ5214	One Type of Positive Photoresist
CBO	Conduction Band Offset
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DIBL	Drain Induced Barrier Lowering
EBL	Electron Beam Lithography
ECV	Electrochemical Capacitance-Voltage
EDS	Electron Dispersion Spectroscopy
EOT	Equivalent Oxide Thickness
FET	Field Effect Transistor
FUSI	Fully Silicide
GWP	Gross World Product
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
InGaAs	Indium Gallium Arsenide (In this work, Indium is 53% if not mentioned otherwise)
IPL	Interfacial Passivation Layer
ITRS	International Technology Roadmap for Semiconductors
MBE	Molecular Beam Epitaxial
MOCVD	Metalorganic Chemical Vapor Deposition
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PDA	Post-Deposition Anneal

PMMA	Poly-methyl-methacrylate
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
SCE	Short Channel Effect
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
VBO	Valence Band Offset
XRD	X-Ray Diffraction
XPS	X-ray Photoelectron Spectroscopy

Chapter 1 : Introduction

1.1 Background

Since the first semiconductor transistor was invented by Bardeen, Brattain and Shockley in 1947 and the first IC (Integrated Circuits) was demonstrated on Germanium by Kilby in 1958, the semiconductor industry has gone through an evaluation at an incommensurable speed for half a century. At present, semiconductor technology is the foundation of many modern civilizations. It forms the basis of the rapid growth of the global electronic industry which is now the largest industry in the world. It is predicted that the semiconductor and electronic industry will continue to extend its proportion in the Gross World Product (GWP). By year 2030, the semiconductor industry may reach 1.6 trillion dollars, while the entire electronic industry may reach 10 trillions dollars and constitutes 10% of the GWP [1.1].

All IC chips, from microprocessor to microcontroller circuit, are made of various small units, i.e. the electron device. Nowadays, the number of transistors integrated in a single IC chip has been increased to billions, and it is usually denoted as the ULSI era. One of the most important electron devices is the MOSFET (Metal Oxide Semiconductor Field Effect Transistor). Currently, the MOSFET is the main stream device for VLSI or ULSI application. From the advance in MOSFET technology, the state-of-art VLSI or ULSI design can provide many diverse benefits, such as, ultra-fast computation, multiple functionality, low standby power and operating power, etc. From super computing machine such as the IBM Blue Gene, to consumer product such as the i-Pod (one of the popular personal portable electronics) and MEMS gyro circuitry in automobile vehicle (the second largest industry in the world), human civilization greatly benefits from the advance of the powerful IC and MOSFET.

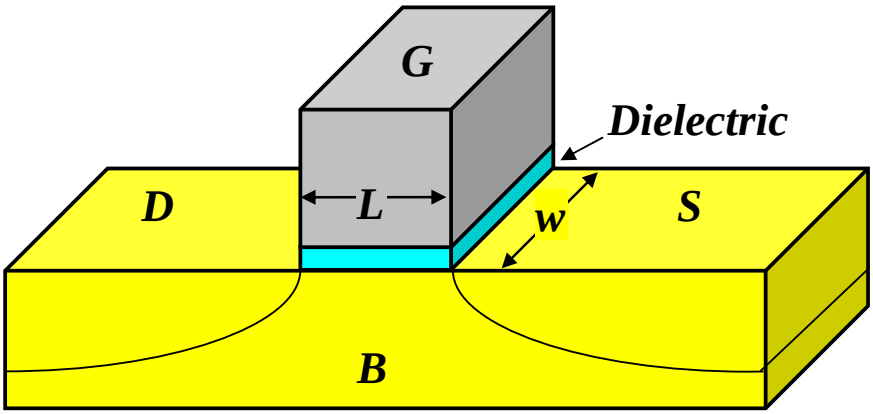

Fig. 1.1 : Schematic of a typical bulk MOSFET structure. Four terminals are denoted as Gate (*G*), Source (*S*), Drain (*D*), and Body (*B*). Geometry parameters are denoted as gate length (*L*) and gate width (*w*). The current flows from drain to source.

The MOSFET is a three- or four-terminal device. The four-terminal bulk MOSFET is shown in Fig. 1.1. The saturated drain current is given by Equation 1.1, where C is the inversion capacitance, $(V_g\text{-}V_{th})$ is the gate overdrive, μ_{eff} is the effective carrier mobility.

$$I_d = \frac{w\mu_{eff}C}{2L}(V_g - V_{th})^2 \qquad (1.1)$$

1.2 Challenge and Motivation

1.2.1 Technology trends

As explained, the revolution of MOSFET technology has been the heart of the IC industry. Scaling of the complementary MOSFET is the driving forces for the increasing IC speed and functionality. Such scaling is vividly described by Moore's law [1.2][1.1]. It was proposed in the 1960s by Gordon Moore, the co-founder of Intel Corporation, that for every 18 months, the size of the transistor will reduce by two

times and the density of devices in a chip will double. The historical trend obeys this exponential scaling law closely as shown in Fig. 1.2.

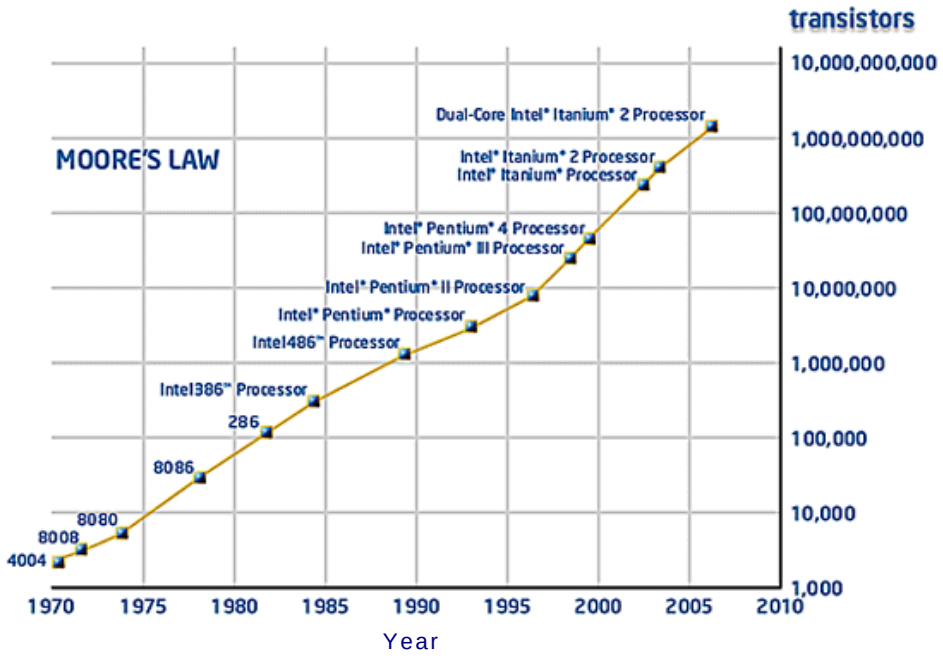

Fig. 1.2 : Historical trend agrees with the Moore's Law. Number of transistor in the Intel Micro Processor increases exponentially over time. It has reached 1 billion in the Dual Core Itanium processor by year 2007. (Source: Intel)

As Moore himself stated in year 2003 [1.4] – No exponential is forever: but "forever" can be delayed. However, there will be increasing challenges of continuing the trend when scaling approaches smaller scale. It requires innovation in both material and device engineering. The international technology roadmap for semiconductors (ITRS), drafted by the world's major semiconductor industry associations, is an assessment of the semiconductor industry's future technology requirements. According to this roadmap, and in actual fabrication, the industry is now moving towards 45 nm technology node. Table 1.1 is extracted from the 2007 ITRS high performance logic requirement [1.5]. To continue the movement to the next generation, such as the 32 nm technology node, most of the technology solutions

required to achieve the expected performance are still not known. To tackle those technological challenges, research of advanced MOSFET becomes extremely imperative.

Table 1.1 : ITRS 2007, from the Process, Integration, Devices and Structures (PIDS) report. It indicates the industry requirement for certain technology node in future. As seen, most of technology solution to reaches 32 nm node in 2013 is still unknown [1.5].

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*28*	*25*
MPU Physical Gate Length (nm)	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
L_g: Physical Lgate for High Performance logic (nm) [1]	*25*	*22*	*20*	*18*	*16*	*14*	*13*	*11*	*10*
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	11	9	7.5	6.5	5.5	5			
UTB FD (Å)				7	6	5.5	5	5	5
DG (Å)					8	7	6	6	6
V_{dd}: Power Supply Voltage (V) [6]									
Extended Planar Bulk (V)	1.1	1	1	1	0.95	0.9			
UTB FD and DG (V)				1	1	0.9	0.9	0.9	0.8
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	134	94	94	103	101	112			
UTB FD (mV)				103	89	87	93	99	99
DG (mV)					115	105	103	108	111
$I_{sd,leak}$: Source/Drain Subthreshold Off-State Leakage Current [8]									
Extended Planar Bulk (µA/µm)	0.34	0.71	0.70	0.64	0.74	0.68			
UTB FD (µA/µm)				0.33	0.52	0.62	0.56	0.55	0.60
DG (µA/µm)					0.2	0.34	0.37	0.38	0.38
$I_{d,sat}$: NMOS Drive Current [9]									
Extended Planar Bulk (µA/µm)	1211	1513	1639	1807	1824	1762			
UTB FD (µA/µm)				1948	2000	1944	2109	2245	2030
DG (µA/µm)					1917	1943	2204	2365	2295
Mobility enhancement factor due to strain [10]	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
$I_{d,sat}$ enhancement factor due to strain [11]									
Extended Planar Bulk	1.09	1.08	1.08	1.08	1.09	1.08			
UTB FD				1.07	1.06	1.06	1.06	1.05	1.05
DG					1.04	1.04	1.04	1.03	1.03

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

1.2.2 Performance boosters

Along with scaling, various technology boosters, such as high-k dielectric, metal or FUSI gate electrode and the transport-enhanced channel, are necessary to control short channel effect (SCE) and maintain continuous performance enhancement.

Silicon dioxide (SiO_2) has been an ideal material as a gate dielectric for Silicon based MOSFET for several decades. However, to control SCE in extremely small devices, the roadmap requires an equivalent oxide thickness below 1 nm. It is not practical to continue using SiO_2 because the gate leakage density will become intolerable for thin oxides. High-k dielectric enables the scaling of equivalent oxide thickness (EOT) with a realistic dielectric physical thickness. There has been a long history of research for high-k dielectric used in silicon MOSFET and such gate dielectric materials will be introduced in industry fabrication very soon [1.6].

Conventional poly Silicon gate suffers from the poly depletion effect. This increases the EOT and compromise the gate to channel electrostatic coupling. Increasing the doping can minimize the poly depletion effect but Boron penetration will occur and cost threshold voltage instability problem. This can be solved by replacing the poly gate by metal or Fully Silicide (FUSI) gate. And the metal gate will be introduced along with high-k dielectric to form the next generation of transistor gate stack [1.9].

In current CMOS technology, the I_{on}/I_{off} ratio is a commonly evaluated merit. It has direct impact on the static power consumption which is critical to Low Standby Power (LSTP) applications. However the subthreshold current for the conventional CMOS device is mainly attributed to the source carrier diffusion current. So the I_{on}/I_{off} ratio is painfully constrained by the limit of 60 mV/dec subthreshold swing (S.S.). This has led to the quest for a switching device having sharper S.S. to achieve a better I_{on}/I_{off} ratio. Innovative device concepts have been proposed for such a purpose. The impact-ionization MOS transistor is one example [1.12].

Strained-Silicon channel has been proven to be useful to improve the saturation drain current in situation where the inversion carrier mobility is serious degraded by

heavy doping in the vicinity of the channel and the use of high-k dielectric. Strained-Silicon has already been successfully integrated into the industrial fabrication process to enhance channel mobility and IC performance. This is a result of great research interests in strain engineering in Silicon, such as, the adoption of multiple process-strained Silicon technique [1.15], high stress Silicon-nitride etch-stop liner [1.16], stress memorization technique [1.17] and the combination of source/drain stressors and strain-transfer structure [1.18]. However, aggressive gate pitch scaling for the purpose of higher circuit density results in the diminished performance gain from various strain engineering schemes. Performance gain degradation associated with stress loss due to pitch scaling will be considerable when the technology generation progresses from the 45 nm node to the 32 nm node [1.20]. As the manufacture of IC devices approaches the 32 nm technology node, researches for future devices that has diminishing dimension in conventional Silicon MOSFET structure are facing many obstacles. To tackle those problems, it calls for the exploration of new materials and device structures to extend the Silicon CMOS scaling.

In deep submicron devices, the thermal injection of carriers from the source into the channel poses a limit for the maximum saturated drain current. This can be overcome by incorporating a more efficient carrier injecting material [1.21]. Considerable interest has been directed towards channel engineering using materials with lower effective mass and high intrinsic carrier mobility, such as Germanium and III-V compounds. The properties of several semiconductor materials are shown in Table 1.2 [1.22].

Germanium has a high mobility for electrons and holes. The Germanium p-MOSFET has been studied extensively [1.23]. However, there are a lot of difficulties in fabricating Germanium n-MOSFET. On the other hand, several types of III-V

compound semiconductor materials have outstanding electron transport characteristics. For example, the lowly doped Indium Gallium Arsenide (InGaAs) material has bulk mobility 9 times (Indium = 53%) higher than Silicon, although the hole motility is very low. Shown in Fig. 1.3, it is expected that in about 10 years' time, the alternative channel material such as InGaAs and Ge will be required for CMOS logic to achieve the desired intrinsic delay [1.25].

Table 1.2 : Common semiconductor materials properties, including electron and hole mobility, lattice parameter and bandgap. Ge has high electron and hole mobility over Si. III-V compounds usually have high electron mobility. But they also have larger lattice constant, resulting in significant lattice mismatch with Silicon.

	Si	Ge	GaAs	InAs	InP	InSb	$In_{0.53}Ga_{0.47}As$
μ_e (cm^2/Vs)	1400	3900	9200	40000	5400	77000	12000
μ_h (cm^2/Vs)	450	1900	400	500	200	850	300
Lattice constant (A)	5.431	5.65	5.653	6.058	5.86	6.48	5.87
Band gap (eV)	1.12	0.66	1.421	0.36	1.34	0.17	0.74

Sadana proposed a CMOS design by using InGaAs for n-channel MOSFET and Germanium for p-channel MOSFET [1.26]. Ge has relatively higher mobility than Silicon for both electron and hole. Sadana's proposal takes advantage of the relatively mature Ge p-FET technology, and potential n-FET performance of GaAs and InGaAs. Sadana's vision of IC structure illustrated in Fig. 1.4 is expected to achieve a performance which satisfies the future IC high speed requirement. Of course the question will be, where there are some technology solutions that enable the fabrication of CMOS compatible InGaAs n-MOSFET and how is their performance. Thus, the main aim of this thesis is to answer these questions.

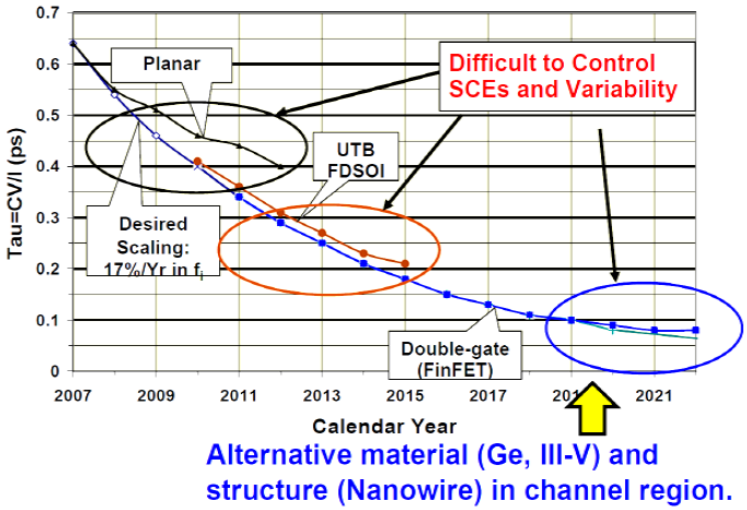

Fig. 1.3 : Expected intrinsic delay requirement versus future years. To achieve sub 0.1 ps performance in year 2019, alternative channel materials such as Ge and III-V are expected to be necessary. (Source: 2007 ITRS Winter Public Conf.)

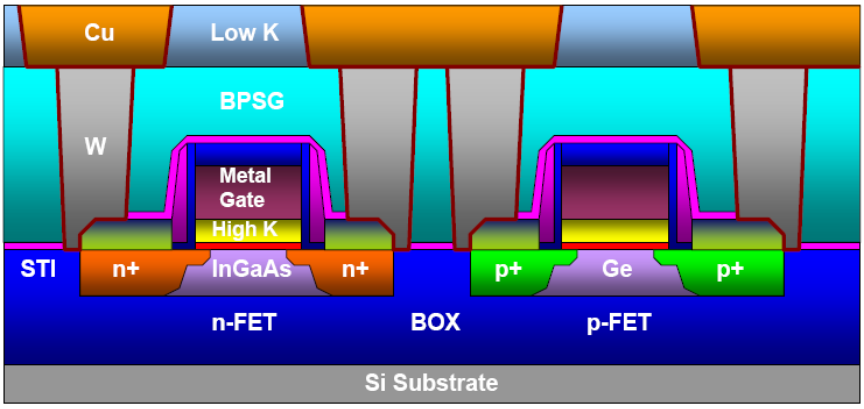

Fig. 1.4 : A schematic showing a possible combination of technology boosters. In the front end, device has high-k dielectric, metal gate electrode, thin body, high mobility InGaAs for n-FET and Ge for p-FET. The back end interconnect includes low-k dielectric and low resistive metal Cu. [1.26]

1.3 Objective

Since long time ago, there has been many works done on n-channel III-V FET. These were mostly used in communication application, power devices and so on. The advantage is that such works provide a relatively mature technology reference to

develop or modify the III-V devices to make it suitable for logic IC purposes. Comparing to some emerging materials, such as graphene, the study of III-V materials for logic has been greatly benefited from traditional III-V devices, such as high electron mobility transistor (HEMT). Kim has first done the analysis of InGaAs channel HEMT for the figure of merits for logic application, such as the intrinsic gate delay and I_{on}/I_{off} ratio [1.27]. Promising results are shown from the deeply scaled HEMT and provide insights to the application of such materials for logic device. The $In_{0.7}Ga_{0.3}As$ Quantum Well (QW) transistor, similar to the HEMT, is successfully integrated onto the Silicon platform in 2007 [1.28], indicating a breakthrough that the total integration of high performing III-V devices on the hetero epi-structure above Silicon platform is possible. Besides, the well-studied metal-semiconductor contact technology has provided very good reference to make the terminals of the devices.

However, III-V devices are not historically studied for CMOS based application. So it is likely to have discrepancy when the silicon CMOS compatibility comes into the picture. Many HEMT devices in the above study [1.27] use the $In_{0.52}Al_{0.48}As$ gate barrier and high workfunction Pt/Au Schottky gates. Such design results in substantial gate leakage when the Schottky gates are forward biased. It also poses challenges in material engineering for CMOS compatibility because Au introduce deep level trap in Silicon. Usually Au is not a favorable material in the front end fabrication. The flatband-mode MOSFET tackles the first problem by introducing an oxide dielectric between the metal gate electrode and $In_{0.52}Al_{0.48}As$ barrier [1.29]. However, a high workfunction metal, such as Au, is still required to turn off the “normally-on” channel. The first inversion-mode InGaAs MOSFET is demonstrated by the gate-last process, Au alloy gate electrode and Atomic Layer Deposition (ALD) gate dielectric [1.31]. Au also poses another problem in process. The inert metal is not easily etched away.

There are not volatile by-products to sustain the etching. So it uses lift-off to define the gate. Nevertheless, impressive channel mobility which is much higher than the universal mobility curve of Silicon is reported. Recently, the self-aligned inversion-mode InGaAs MOSFET is demonstrated, featuring high CMOS compatibility [1.33].

The conventional MOS gate stack is made by high temperature thermal oxidation of Silicon to form SiO_2. The native oxide of Silicon is very stable and forms good interface with Silicon. However, almost all high mobility materials do not have chemically stable native oxide and good interface. For example, Arsenic oxide has a very low boiling point, and Germanium oxide is very vulnerable. The lack of a stable native oxide for most high mobility materials has been a major obstacle for MOS fabrication. In the MOSFET performance, the concern of interfacial quality between the directly deposited high-k dielectric and III-V channel is embodied in the unsatisfied subthreshold swing [1.32]. It usually requires advanced interface engineering between deposited dielectric and substrate. Extensive study has been carried out for Ge and GaAs. Take GaAs for example, AlN passivation, plasma nitridation and Si passivation have been used, otherwise serious Fermi level pinning is observed [1.34]. With these efforts, GaAs n-MOSFETs have been demonstrated [1.38].

If one looks at the big picture, a key step to realize such integration is to make all the above-mentioned devices on the Silicon platform. This depends on the material engineering advance – high quality single crystalline III-V film to be grown or bonded on Silicon. In fact, many studies have been directed into this research. Its application is not only limited for the front end devices, but also benefits other on-chip functions, such as optical interconnect, waveguide and detector. As shown in Table 1.2, most III-V materials have a significant lattice mismatch with Silicon. Usually a compositional

grading layer is required for integration. III-V integration with Silicon for future VLSI circuits has become a hot topic and promising progress has been made [1.42].

As introduced, metal gate, high-k dielectric and high mobility III-V channel are attractive technology boosters for future CMOS devices. The first objective of this project is to explore the integration of the above mentioned technology boosters with CMOS compatibility. From the materials perspective, gate stack grown by normal CVD and sputter/etch is free of Au and suitable for front end integration. From the process perspective, the top-down fabrication approach and self-aligned source and drain are most similar to the present CMOS; its fabrication should allow the device to be easily scalable as the Silicon CMOS devices. Secondly, the device should exhibit significant performance enhancement than Silicon in some of the figures of merit for logic. InGaAs is shown to be a good candidature from the III-V family for n-MOSFET application. The interface between the deposited high-k dielectric and III-V substrate will be studied extensively. Further interface engineering techniques will enhance the device's performance. This work is mainly based on the lattice matched InGaAs on InP substrate. Total integration with Silicon is not covered in this thesis as it is expected to be a future work where the high performing III-V MOSFET and III-V on Silicon technologies will eventually converge.

1.4 Outline of the Thesis

Chapter 2 describes the process integration. Activation of implanted InGaAs is studied by various rapid thermal annealing conditions. Two keys properties are studied: the rectifying characteristic of the p-n+ junction and conducting characteristic of the n+ region. Hafnium based high-k dielectric is deposited by MOCVD. The

physical and electrical properties of the gate stack are studied. With a self-aligned process, bring all parts above together, the InGaAs channel MOSFET with directly deposited HfAlO is fabricated and investigated.

Chapter 3 focuses on the interface engineering using *in-situ* plasma Phosphor passivation. This work reports on the fabrication of the InGaAs MOSFET with calibrated surface passivation. Tremendous performance enhancements are reported. The physical and electrical properties of the MOS devices are investigated and compared with the directly deposited control devices.

Chapter 4 describes the fabrication of sub-micron short channel MOSFET. Necessity and challenge to achieve sub-micron gate length MOSFET are summarized. Small dimension is realized by electron beam lithography. An innovative process is then proposed to overcome the long time required for the serial process. Gate pattern of 40 nm is performed using this method. The sub-micron MOSFET is demonstrated with high performance. The impact of source and drain series resistance to further MOSFET scaling is analyzed.

Chapter 5 summarized the result drawn from this work and made suggestion for future study.

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Chapter 2 : Fabrication of InGaAs MOSFET

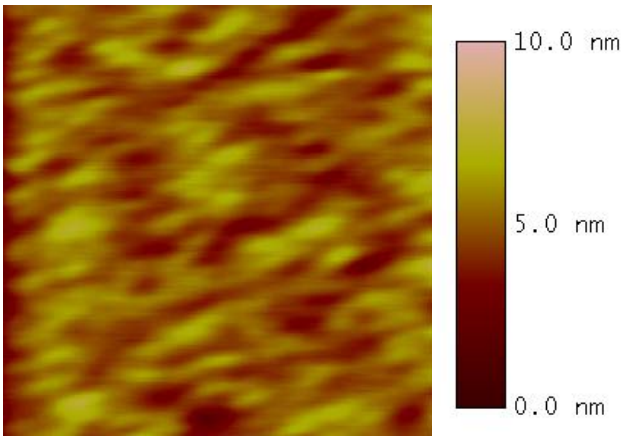
2.1 Introduction

Recently, the inversion-mode $In_{0.53}Ga_{0.47}As$ n-MOSFET was successfully demonstrated. It employed the gate-last process and exhibited high electron mobility in the inversion channel [2.1]. The gate last process serves the purpose of reducing the thermal budget after the gate dielectric growth. This is favorable for the integration with high-k dielectric in CMOS process. However, gate-last process introduces fabrication complexity during the masks alignment. The gate and source/drain misalignment could result in higher series resistance and loss in the drain current.

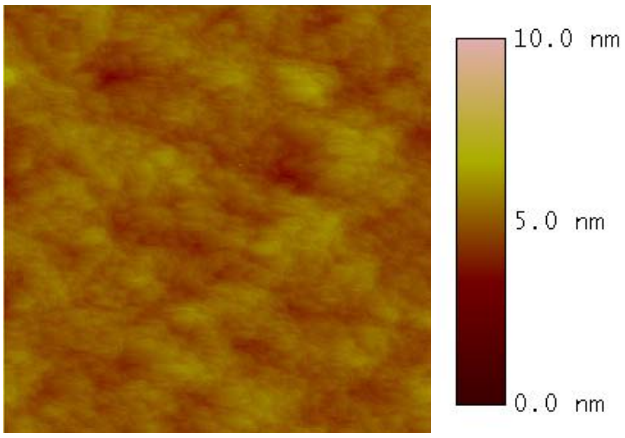
In this chapter, a self-aligned gate-first InGaAs MOSFET fabrication process is introduced. Beginning with lattice matched InGaAs grown on InP, the surface chemistry of InGaAs is compared with GaAs. Then two unit processes are studied: MOS gate stack integrity, source and drain activation. The MOSFET is then fabricated and analyzed. Work reported in this chapter has resulted in a journal publication [2.2].

2.2 Growth of Substrate

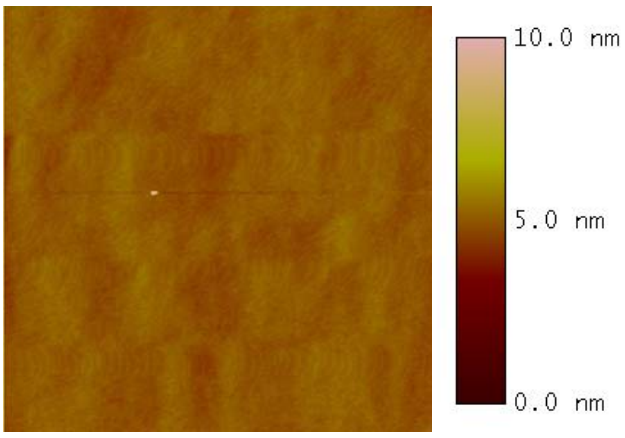
At the beginning of the project, InGaAs grown on GaAs (Indium = 20%) and InP (Indium = 53%) were carried out by Molecular Beam Epitaxial (MBE). Three experiments were dedicated to develop the recipe. $In_{0.53}Ga_{0.47}As$ was grown on 2-inch p^+ InP substrate (doping level was $3x10^{18}$ cm^{-3}). During the growth, the fluxes of precursors were controlled in real time. The film on GaAs and InP in the best experiment were measured as shown in Fig. 2.1 with the growth specification indicated below each figure.



(a) RMS=0.856 nm (15 nm InGaAs on GaAs, undoped, Run 2 #2, 2007-10-17)



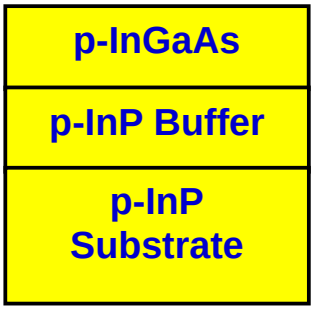
(b) RMS=0.373 nm (30 nm InGaAs on InP, undoped, Run 2 #1, 2007-10-17)



(c) RMS=0.223 nm (30 nm InGaAs on InP, p-doped by Be, Run 2 #2, 2007-10-17)

Fig. 2.1 : AFM images of surface topology for MBE grown samples. The scanning areas are 5x5 um^2. The surface RMS roughness values are indicated for each sample. (a) 15 nm undoped $In_{0.15}Ga_{0.85}As$ growth on p-GaAs. substrate (b) 30 nm undoped $In_{0.53}Ga_{0.47}As$ on p-InP. (c) 30 nm Be doped $In_{0.53}Ga_{0.47}As$ on p-InP.

However, the growth conditions in the above three runs showed some instability and non-repeatability problems. Meanwhile, low throughput, long time of preparation and costly growth limited the study of device fabrication. The above experimental runs only grew a thickness of a few tens of nm even for lattice matched InGaAs on InP. Generally, a thickness of a few hundreds of nanometer is required for MOSFET fabrication and the time of growth would be even longer. Also, the doping could not be controlled and extracted very accurately. The following experiments for MOSFET fabrication used the commercially growth InGaAs wafer.



InGaAs (500nm, Zn doped $1x10^{17}$ cm^{-3}).

InP buffer (Zn p^+)

InP Substrate (Zn p^+)

Fig. 2.2 : Specification for MBE growth of p-InGaAs on InP. An InP buffer is first grown, followed by InGaAs. InGaAs is 500 nm thick, lattice matched with InP.

MBE substrates from commercial growth services are described as follows. On a 2-inch p^+ InP substrate (doping level was $3x10^{18}$ cm^{-3}), 200 nm p-doped InP buffer and 500 nm p-doped $In_{0.53}Ga_{0.47}As$ were sequentially grown by MBE. Above mentioned p-type dopants were Zn and doping level was extracted by the electrochemical capacitance-voltage (ECV) method. The ECV profiling technique provides a quick and accurate evaluation of the concentration and depth distribution of carriers in doped layers. Furthermore, it was confirmed that the $In_{0.53}Ga_{0.47}As$ epitaxial layer was strain-free by X-Ray diffraction (XRD) measurement. Growth specification as well as the finished structure is shown in Fig. 2.2. A relatively thick

InGaAs is used, and mainly serves two purposes. Firstly, the doping is reduced gradually from the buffer layer to the top surface of InGaAs. A lower doping is desirable. Secondly, a thick layer of over 400 nm is required to ensure the subsequently fabricated devices are located in the conformal InGaAs layer.

In addition, there are two types of epitaxial structure which have been grown in this work as shown in Table 2.1. Type-2 is only available very recently with a more accurate growth control for surface roughness and doping level. The device made on Type-2 substrate has shown improved performance as will be discussed in the later sections. However, most of the study in this work since year 2007 utilizes Type-1 substrate. It is the substrate to be used for device fabrication unless otherwise mentioned.

Table 2.1 : Two types of substrate and their specifications. Type-1 substrate is the main source of study in this work. Type-2 substrate has a lower doping level and exactly orientated surface which is available for the more recent study.

Substrate	Surface doping level	Starting substrate	Time of application
Type 1	$1x10^{17}$ cm^{-3}	(100) +/- 0.2^{o}	2007 Oct. - present
Type 2	$1x10^{16}$ cm^{-3}	(100) +/- 0.05^{o}	2009 Mar. - present

Control of the surface doping level is one of the critical issues in the growth stage. A lower doping is desirable to alleviate the impurity scattering and beneficial for the high mobility nature of InGaAs. The lowest level of doping is limited by the control of growth process and resolution of characterization of actual dopant profile. The doping profile for Type-1 substrate is extracted from the ECV method and shown in Fig. 2.3. The doping decreases from the buffer to the interface and surface. The kink between buffer InP and InGaAs is due to the accumulation of dopant in the interface. As the device is mainly located above 200 nm of the surface, the dopant is uniform.

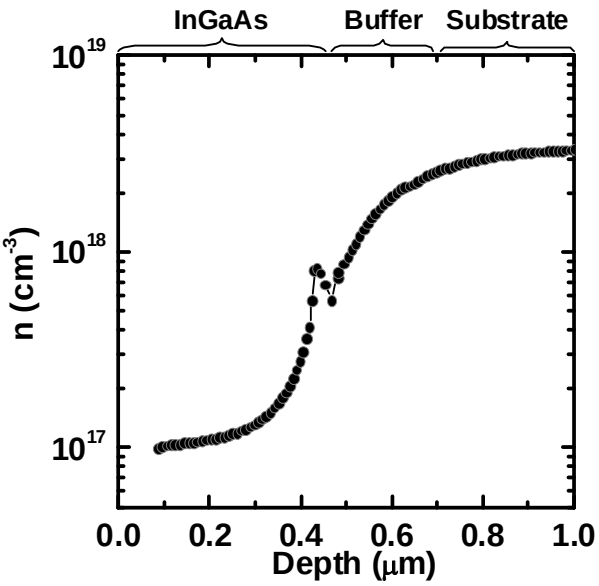


Fig. 2.3 : Doping concentration as function of depth from the InGaAs surface in Type-1 substrate. Near the surface dopant concentration is about $1x10^{17}$ cm^{-3}.

2.3 Directly Deposited High-k on III-V

2.3.1 Surface preparation

As the fabrication of Silicon MOS device, the surface preparation is an important step before growth or deposition of dielectric. Diluted acid is used for surface cleaning, followed by $(NH_4)_2S$ surface treatment. The acid can be either 10% hydrochloric acid (HCl) or 1% hydrofluoric acid (HF), which can remove the native oxide originated from the surface. From the AFM image in Fig. 2.4, HCl cleaning for 2 minutes does not significantly attack the surface (RMS from 0.74 nm to 0.82 nm). AFM images (a) and (b) in Fig. 2.4 show the surface roughness before and after this step, respectively. The surface roughness is only slightly increased by using this chemical treatment. The surface passivation by Chalcogen atoms, such as Sulphur or Selenium, is a method widely adopted in III-V devices [2.3]. $(NH_4)_2S$ treatment has

also been adopted for III-V/high-k MOS device fabrication [2.9]. In this work, 2 minutes HCl acid cleaning, 5 minutes $(NH_4)_2S$ treatment and 3 minutes de-ionized water rinse are the standard pre-gate cleaning procedure.

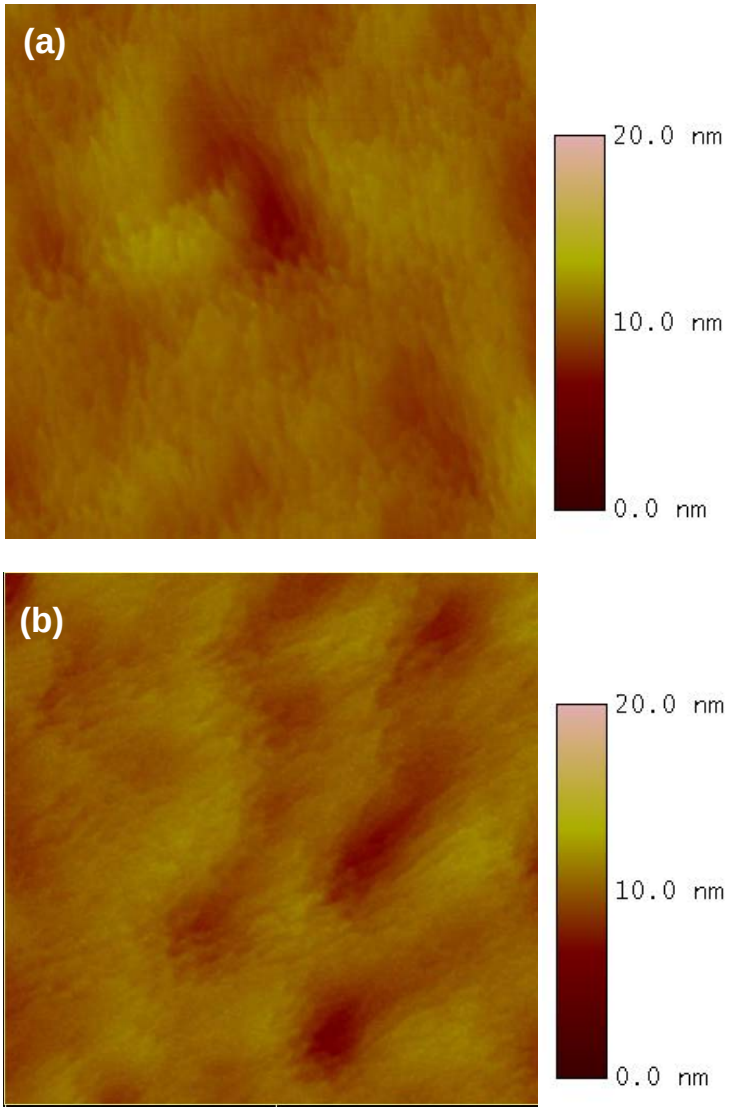


Fig. 2.4 : AFM image of InGaAs of (a) as growth, RMS roughness is 0.74 nm; (b) after pre-gate cleaning and surface treatment RMS roughness is 0.82 nm. Scanning window is 5x5 um^2.

2.3.2 High-k/InGaAs interface study

HfAlO is deposited by MOCVD using $HfAl(MMP)_2(OiPr)_5$ as precursor. It comprised of 10% Al_2O_3 and 90% HfO_2. The advantage of HfAlO over HfO_2 is that

the crystallization temperature is lower for HfAlO. So HfAlO is believed to have a better thermal stability and can be removed by HF to leave the source and drain contact opening after a higher temperature process. So it is choice of dielectric materials in the first experiment. Arsenic oxide is a concern for interface degradation. Experiments are carried out to examine the susceptibility of Ga- and As- native oxide formation for InGaAs and GaAs substrate. The GaAs substrate is also p-type, doped by Zn. Doping level is 1×10^{16} cm^{-3}. After pre-gate cleaning and treatment, both substrates are exposed to atmosphere while transferring to the XPS chamber. During this period, As-O has already formed on the GaAs sample. Fig. 2.5 shows the As-3d peak characterized by the average 5 XPS scans, the profile has been smoothened to eliminate the noise. A clear existent of As-O bond is found at binding energy around 44 to 45 eV.

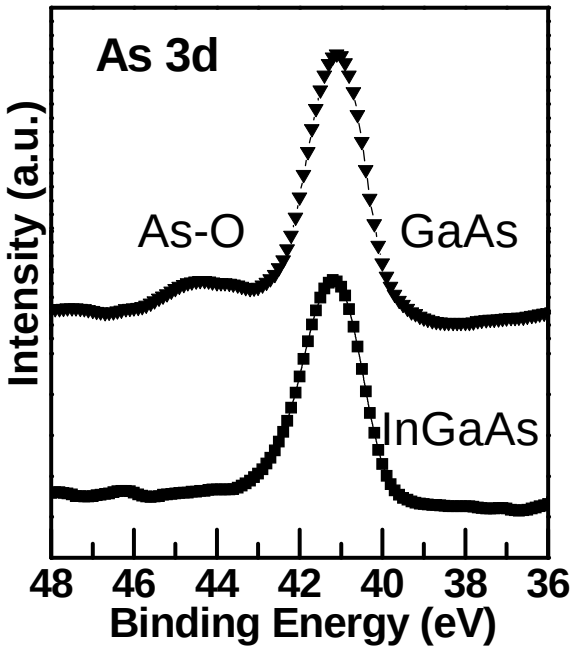


Fig. 2.5 : InGaAs showing a better suppression of As-O formation comparing to GaAs. After pre-gate cleaning and exposed to atmospheric ambient, the XPS scan of As-3d peak is shown. A clear As-O formation is found in GaAs sample and it is not detected on InGaAs.

Then a further exploration using high resolution XPS which enables more scanning cycles is carried out. This time, a very thin layer of MOCVD HfAlO dielectric is deposited on GaAs and InGaAs immediately after the cleaning. The purpose is to explore the integration of InGaAs and GaAs with HfAlO. The O-1s peak is obtained in Fig. 2.6. After decomposition of the O-1s peak according to the oxygen to existing element binding energies, it is found that, Ga- and As- native oxide formed on GaAs, while InGaAs does not show a detectable Ga- and As- oxide peak. The Indium in the III-V substrate helps in the integration with HfAlO dielectric. This can be one reason that most GaAs MOS devices usually suffer from the serious Fermi level pinning unless an interface passivation layer is used [2.11]. But in this work, InGaAs MOS device is possible using directly deposited high-k.

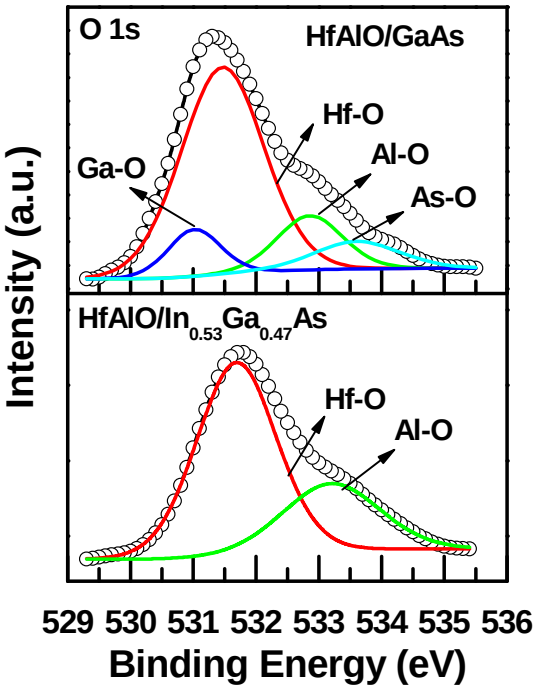


Fig. 2.6 : InGaAs showing a better suppression of As-O formation comparing to GaAs. After a thin layer (2 nm) of HfAlO deposition and PDA, high resolution XPS scan of the Oxygen 1s-peak shows clear native oxide of As and Ga on the GaAs sample, while such native oxide components are not detectable on InGaAs sample.

2.3.3 Band alignment

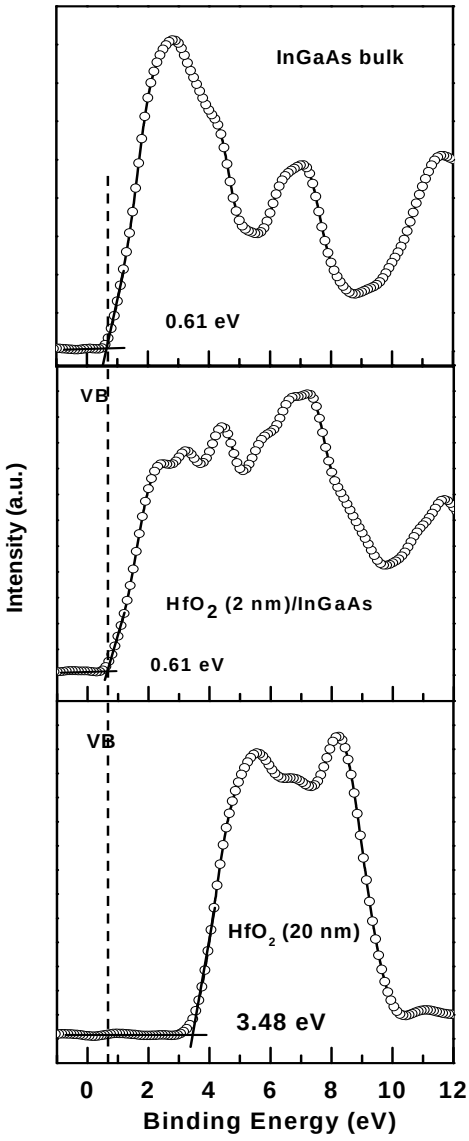


Fig. 2.7 : Valence band spectra of p-InGaAs bulk and HfO_2 film deposited on p-InGaAs.

The band alignment of MOCVD high-k dielectric and InGaAs can be measured from Valence Band (VB) spectra method [2.13]. The experiment includes three samples for XPS: (1) bulk p-InGaAs, (2) thin HfO_2 on p-InGaAs (3) thick HfO_2 on p-InGaAs. Fig. 2.7 shows the VB spectra for bulk p-InGaAs and HfO_2/p-InGaAs. The VB edge of bulk InGaAs and thick HfO_2 films on InGaAs were determined to be 0.61 and 3.48 eV, respectively. From this, the effective VBO between HfO_2 and InGaAs is

determined to be 2.87 eV. The effective CBO can be evaluated by subtracting the effective VBO and the band gap of the substrate (0.74 eV) from the band gap of HfO_2 of 5.7 eV. The effective CBO between HfO_2 and InGaAs substrate is 1.99 eV.

The same study was done on HfAlO/InGaAs system as well. The VBO and CBO for HfAlO/InGaAs are 3.29 and 2.37 eV, respectively. The band alignment for HfAlO and HfO_2 are then determined and summarized in Fig. 2.8.

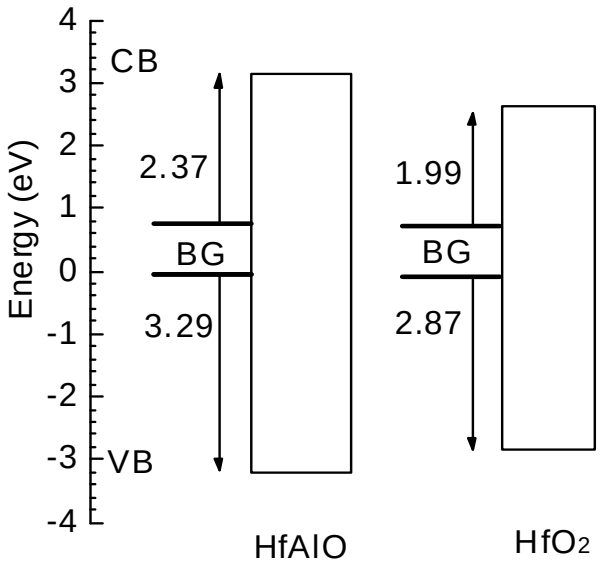


Fig. 2.8 : VB spectra method determined band offset for HfAlO and HfO_2 on InGaAs.

2.3.4 MOS capacitor

TaN holds a promise to replace the poly Silicon gate electrode because it is a metal gate which can be etched by Reactive Ion Etching (RIE). Previous work on InGaAs MOSFET normally use the lift-off method to pattern some high workfunction gate. This is not CMOS compatible as now the major CMOS front end processes are all using a top-down etching approach. Besides, TaN is a good candidate on high-k gate stack. There are researches on the effective workfunction tuning on Silicon MOSFET with TaN/Hf-based gate. Thus, it potentially allows threshold voltage

adjustment in future CMOS fabrication. In this work, Reactive Ion Sputtering of Ta in N_2/Ar ambient is used to deposit TaN on high-k/InGaAs.

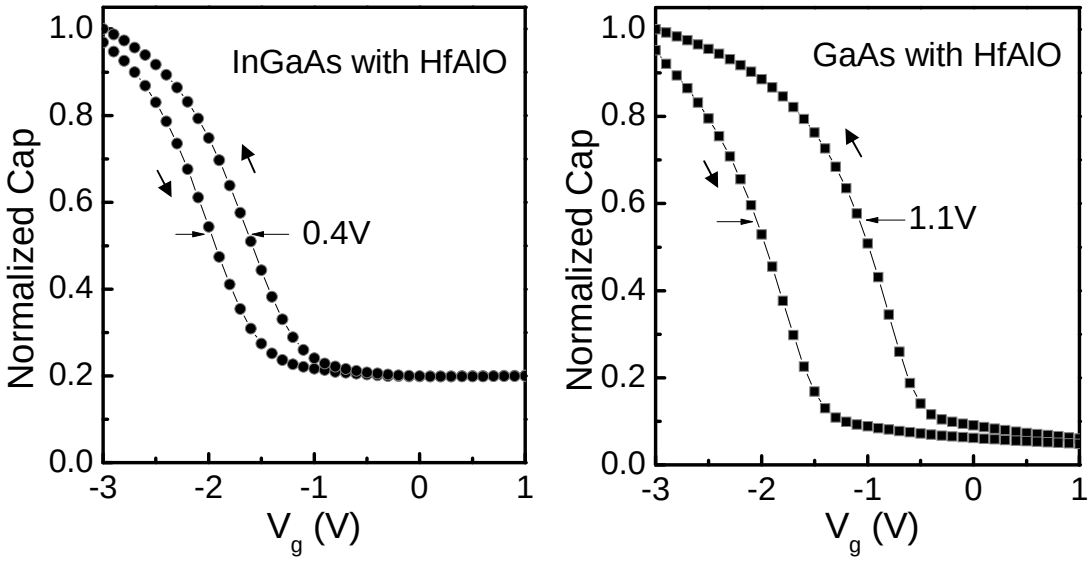


Fig. 2.9 : Normalized capacitance for two MOS systems (a) TaN/HfAlO/p-InGaAs and (b) TaN/HfAlO/p-GaAs. Hysteresis is 0.4 V for InGaAs substrate for and 1.1 V for GaAs substrate. Indium reduces the hysteresis significantly.

The normalized C-V characteristic of a MOS capacitor is studied in Fig. 2.9. The hysteresis of InGaAs MOS capacitor is much smaller than GaAs, both with directly deposited HfAlO as gate dielectric. This indicates that the amount of bulk traps and interface traps for InGaAs MOS system is smaller than that in GaAs. A complete study has been reported in recent publication [2.16]. This agrees with recent reported result with different passivation technique (Silicon passivation) on InGaAs and GaAs MOS devices [2.17].

Leakage level for the MOS capacitor is in the order of 10^{-6} A/cm^2 at gate biases of 2 V. More discussion on gate leakage density will be given in the later part of MOSFET integration.

2.4 Source and Drain Activation

Silicon is n-type dopant for GaAs and InGaAs. To study the source and drain engineering on InGaAs MOSFET, dopant activation experiment is done on the Silicon implanted InGaAs. Two key properties of source and drain in a MOSFET are, the high conducting, i.e. low resistance, characteristic and junction rectifying characteristic. Those two properties can be achieved by a high level of dopant activation in the source and drain. However, high temperature activation causes problem in the process integration such as degrading the high-k dielectric.

This section of experiment is carried out as follows. Silicon is implanted through 10 nm of sacrificial SiO_2 into the InGaAs with dose of 1×10^{14} cm^{-2} and energy of 50 keV. Then with a 100 nm SiO_2 capping layer, the sample then goes through various activation conditions. The RTA system is a standard setup for 8-inch Silicon wafer. The InGaAs sample is put on top of a dummy 8-inch Silicon wafer where temperature is monitored by a Pyrometer. After RTA, the SiO_2 capping is removed. The contact is then made by photolithography and electron beam evaporated AuGe/Ni/Au alloy. In some case, electron beam evaporated Pd is also applied as contact in the experiment, and it shows comparable electrical contact properties. However, after lift-off, the adhesion of Pd on InGaAs is not as good as Au and it is easily worn out by probing in experiment. Back contact for junction measurement is also made of Au alloy.

Metal-semiconductor contact resistance R_c and semiconductor film sheet resistance R_{sh} can be measured by four-point probe and the transfer line method (TLM) [2.18]. The TLM pattern is shown in Fig. 2.10. A mask of TLM ladder pattern has been drawn and attached in Appendix 1. The total resistance between two contact pads is given by Equation 2.1, assuming R_{sh} to be identical under the contacts and between contacts. When the total resistance versus distance between two pads is

plotted, R_c and R_{sh} can be obtained. One example of the test result is shown in Fig. 2.11. The linear fitting parameters are slope and intercept with *y* axis. The fitting line follows nicely with the measured data. R_{sh} is obtained from the slope of the fitting curve while R_c is obtained from the intercept with the *y* axis.

$$R_T = \frac{R_{sh}}{Z} d + 2R_c \approx \frac{R_{sh}}{Z}(d + 2L_T) \tag{2.1}$$

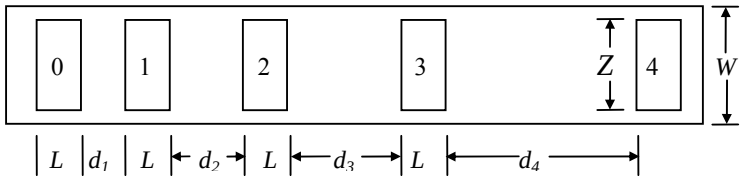


Fig. 2.10 : TLM test structure. Number *n* (0, 1, 2…) denotes the contact number. d_n denotes the distances between two adjacent contact pad. *Z* is the width of the contact.

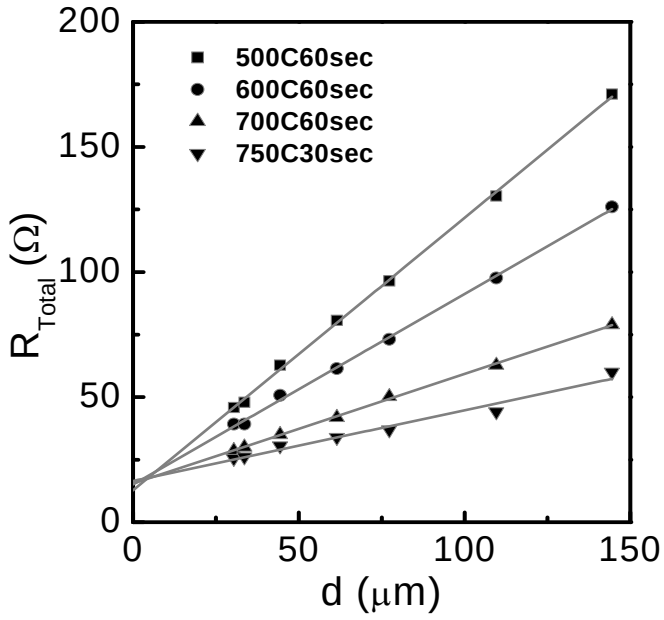


Fig. 2.11 : Total resistance versus distance. TLM test results for implanted samples which are activated at different conditions. Two linear fitting parameters are slope and intercept with the *y* axis.

Fig. 2.12 shows the sheet resistance of Silicon implanted InGaAs after various RTA processes: 500 ^oC to 700 ^oC for 60 sec, 750 ^oC for 30 sec and 800 ^oC for 10 sec.

Firstly, R_{sh} is measured from four-point probe in different location across a sample of size 1x1 cm^2. The scale bar indicated the maximum and minimum records and the bullet indicates the mean value of all data points. The number of sampling points varies from 8 to 15. It is observed that sheet resistance is reducing tremendously before annealing temperature of 600 ^oC. This is similar to the result measured by the TLM test. However, at elevated temperature such as above 750 ^oC, there is a discrepancy between R_{sh} measured by TLM and four-point probe measurement. By RTA 600 ^oC for 60 sec, R_{sh} of the Silicon implanted n^+ region was around 65±15 Ω/□. However, when RTA temperature is above 850 ^oC for 30 sec, the temperature is high enough to cause damage on the samples. The damage includes crack and void on the samples that appear after high temperature RTA. In Fig. 2.11, all curves have intercepts with the *y* axis at a same point, indicating $2R_c$. The contact resistance R_c is determined to be around 0.6 Ω.mm.

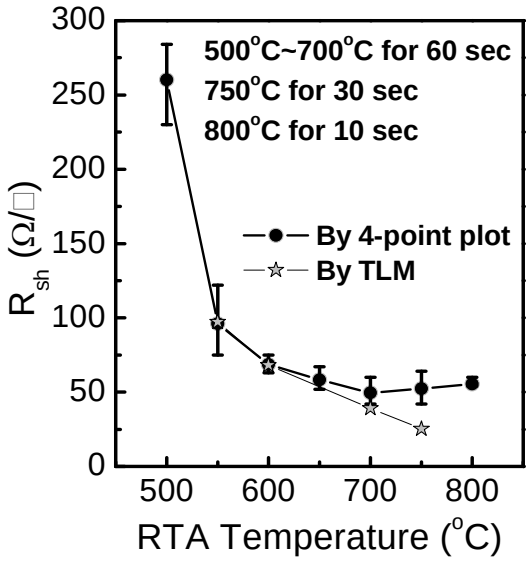


Fig. 2.12 : Sheet resistance in various activation condition, measured by both four-point probe and TLM method.

Good rectifying n^+-p junction, measured between the S/D contact and back contact, is achieved in Fig. 2.13. Forward current and reverse current ratio is 6 orders. This significantly reduces the junction leakage when the transistor is in standby state. Previously GaAs inversion-mode MOSFET uses an activation temperature of higher than 750 ^oC [2.19]. This work reveals that low thermal budget of the InGaAs MOSFET activation process is possible. This may be explained by the higher Gibbs free energy of InAs than GaAs, and Si dopants are easier to enter the Indium substitutional sites. This can help to mitigate the thermal constraint of metal/high-k gate stack and beneficial for the MOS devices.

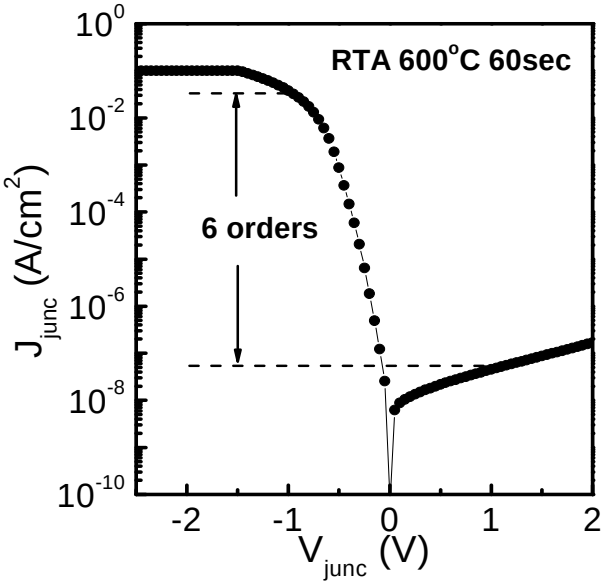


Fig. 2.13 : Junction current versus the voltage across n^+/p junction applied between the implanted source/drain and the substrate in InGaAs n-MOSFET.

2.5 MOSFET with Directly Deposited HfAlO

2.5.1 Process integration

All above topics in this chapter include substrate growth, surface preparation, gate stack integration, Silicon activation in InGaAs. They are modular experiments prepared for the integration of a transistor.

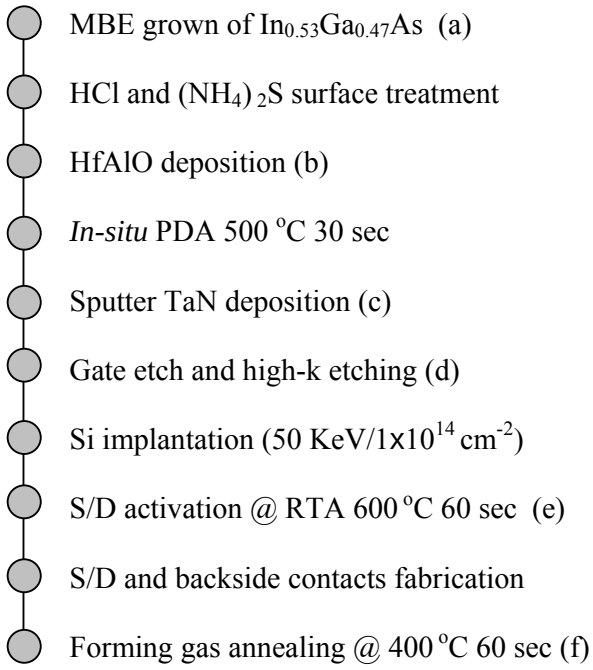


Fig. 2.14 : Process flow of fabricating InGaAs n-MOSFET. Process steps (a-f) are described by a cross sectional schematic diagram in next figure.

Fig. 2.14 is the process flow and Fig. 2.15 is the cross section schematic of the structures in some key steps. This fabrication method followed the self-aligned approach for the n-channel InGaAs MOSFET. After standard substrate cleaning, the wafers were transferred to the MOCVD reactor immediately. HfAlO was grown at 425 °C using ($HfAl(MMP)_2(OiPr)_5$) source, followed by the *in-situ* post-deposition anneal (PDA) at 500 °C in N_2 ambient for 30 sec. Subsequently, TaN metal gate electrode was deposited by Reactive Ion Sputtering Ta target in Ar/N_2 gas. Optical

lithography is used to define the gate pattern and Chlorine gas based dry etch of TaN is applied. HfAlO is etched by 1% HF in subsequent process, aligned to the gate. Then a thin SiO_2 sacrificial layer was deposited on the wafer before the source and drain region were selectively implanted with Silicon at a dose of $1x10^{14}$ cm^{-2} at 50 KeV. Implantation activation was achieved by rapid thermal annealing (RTA) at 600 ^oC for 60 sec in N_2 ambient. Subsequently, AuGe/Ni/Au and Ti/Pd/Au were deposited to form the front source/drain contacts and the backside contact, respectively, followed by RTA at 360 ^oC for 60 sec in N_2 ambient. Lastly, the forming gas annealing was performed at 400 ^oC for 60 sec.

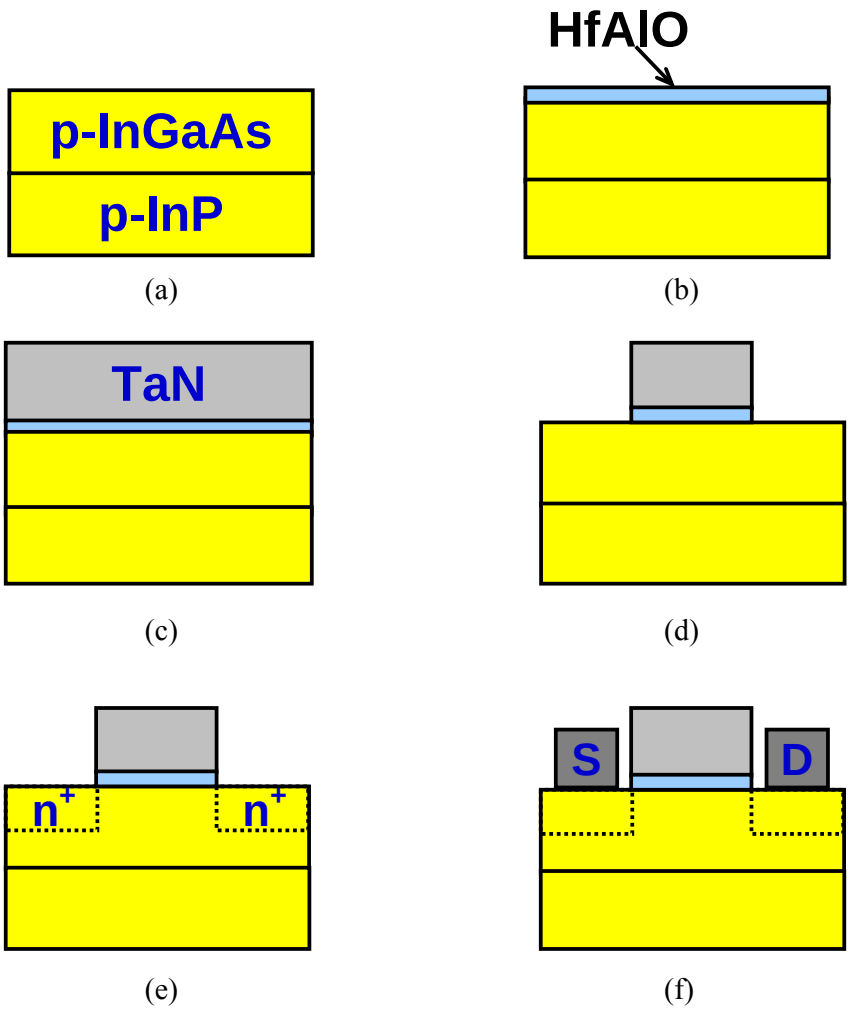


Fig. 2.15 : Cross sectional schematic of self-aligned InGaAs MOSFET fabrication. (a) – (e) are the intermediate steps and (f) is the final device structure.

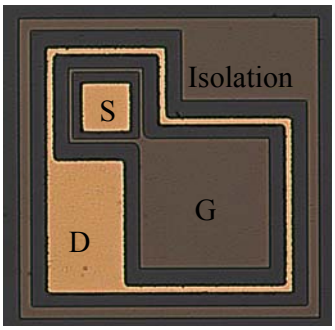


Fig. 2.16 : Top view of a ring-shape gate InGaAs MOSFET. This transistor is fabricated with a two-mask step.

This is a two-mask transistor process. One mask is for ring-shape gate pattern and device isolation. Another mask is for the source and drain contact pattern. The ring-shape gate separates the source and drain as shown in Fig. 2.16. Device isolation is achieved by the outside ring which places a back-to-back diode between the drains of adjacent devices.

2.5.2 Results and discussion

HRTEM image in Fig. 2.17 illustrates excellent interface between MOCVD HfAlO and InGaAs. The surface is conformal and with high quality. HfAlO film thickness is 14.1 nm. Within HfAlO film, negligible amounts of In, Ga, and As diffusions were detected by EDS analysis.

Gate leakage current density versus different gate bias is shown in Fig. 2.18, measured with source, drain and substrate grounded. At a gate bias of ±2 V, the gate leakage density was below 10^{-6} A/cm^2, similar to the lowest reported gate leakage of CVD HfO_2 on GaAs with various interface passivation layers (IPL) and comparable equivalent oxide thickness (EOT) under the same gate biases [2.10]. The low leakage currents of TaN/ HfAlO/ InGaAs gate stacks for both gate and substrate injection

cases can be attributed to the high conduction band offset (CBO) and valence band offset (VBO) between HfAlO and InGaAs channel which are reported in the previous section.

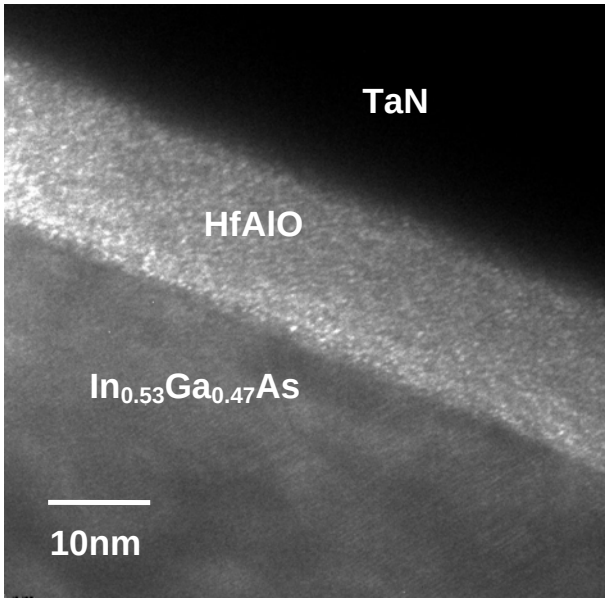


Fig. 2.17 : A cross section of an inversion-mode self-aligned $In_{0.53}Ga_{0.47}As$ n-MOSFET with CVD HfAlO gate dielectric and TaN metal gate.

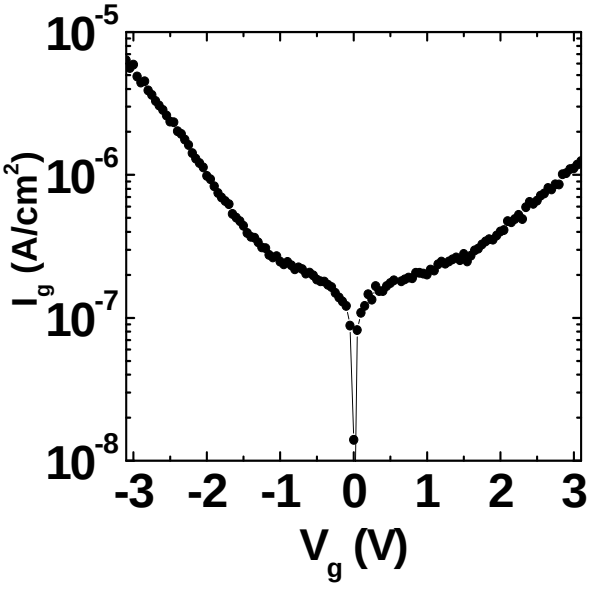


Fig. 2.18 : The gate leakage current density versus the voltage applied to the gate with source, drain and backside electrode grounded for the fabricated InGaAs n-MOSFET.

HfAlO/TaN gate stack integrity is illustrated in Fig. 2.19. It shows that well-performed inversion gate to source/drain capacitance is achieved. The C-V characteristic between gate and tied-up S/D shows excellent inversion characteristics for MOSFET turn on operation. Note that the capacitances are measured from MOSFET after RTA S/D activation and forming gas annealing. It turns out that after 600 ^{o}C annealing, the gate stack maintains stable. EOT was 4.25 nm, extracted from the accumulation capacitance-voltage measurement. It is fitted with the simulation curve considering quantum mechanical (QM) effect. D_{it} value was determined to be $3x10^{12}$ $cm^{-2}eV^{-1}$.

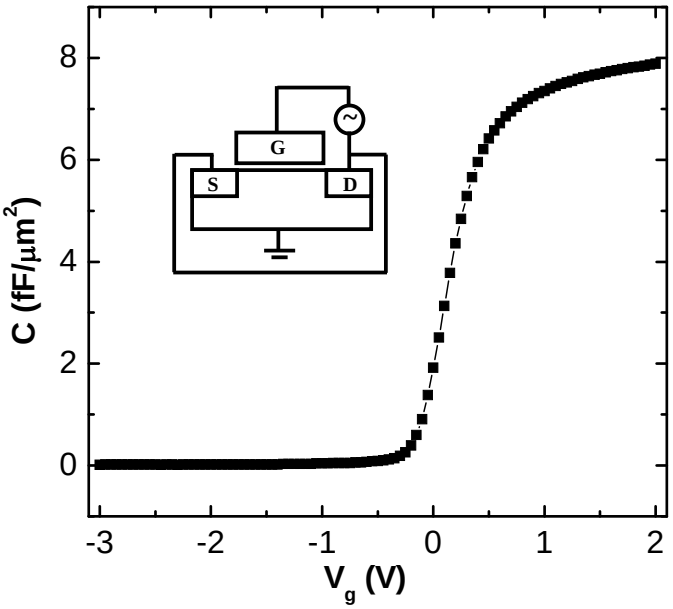


Fig. 2.19 : Inversion capacitance versus applied gate bias. Inversion capacitance measures the high frequency capacitance (100 kHz) between gate to source and drain with substrate grounded as shown in the inset schematic.

Fig. 2.20 shows the well-behaved subthreshold performance of the fabricated $In_{0.53}Ga_{0.47}As$ n-MOSFET with gate length of 4 μm, at drain biases of 1 V and 50 mV respectively. The drain induced barrier lowering was 68.1 mV/V for this device.

Considering the bandgap of $In_{0.53}Ga_{0.47}As$ is 0.74 eV [2.22], it is predicted that using a low bandgap material as channel, the source to drain leakage contributes a significant off-state leakage current due to the thermal generation of minority carriers [2.23] and band to band tunneling. The on-current over the off-current at V_g = -1 V is over 4 orders for this device, similar to that reported in Ref. [2.24]. Subthreshold swing was 196 mV/dec. Nevertheless, the threshold voltage in this device is close to zero which causes an off-current at V_g = 0 V relatively high for enhancement operation. Although high workfunction Au alloy can help to achieve higher threshold voltage [2.1], Au is currently not a Silicon CMOS compatible material.

Fig. 2.21 shows the linear scale I_d-V_g of the 4 μm gate length $In_{0.53}Ga_{0.47}As$ n-MOSFET at a drain bias of 50 mV and 1 V as well as their transconductances. Maximum gate transconductances were 3.3 mS/mm for V_d = 50 mV and 34 mS/mm for V_d = 1 V.

Fig. 2.22 shows the I_d-V_d curves for the 4 μm gate length $In_{0.53}Ga_{0.47}As$ n-MOSFET measured with V_g from 0 to 3 V in 0.5 V step in a bidirectional drain bias sweeping. It exhibited negligible hysteresis for a wide range of biased voltages, indicating low bulk oxide trapped charges and low interfacial density of states in the HfAlO/$In_{0.53}Ga_{0.47}As$ interface. Well-behaved I_d-V_d characteristics show an enhancement-mode operation.

2.6 Summary

The $In_{0.53}Ga_{0.47}As$ channel n-channel MOEFET is successfully demonstrated with HfAlO as gate dielectric and TaN as metal gate. Self-aligned process is utilized and low temperature activation process is possible due to the high content of Indium,

which is beneficial for high-k gate dielectric. XPS shows that for HfAlO as gate dielectric, InGaAs is more effective to suppress the GaO and AsO formation than GaAs. Excellent I_d-V_d and I_d-V_g characteristics of enhancement mode operation are reported. InGaAs is a promising material for channel engineering for high mobility MOSFET integrated with high-k dielectric.

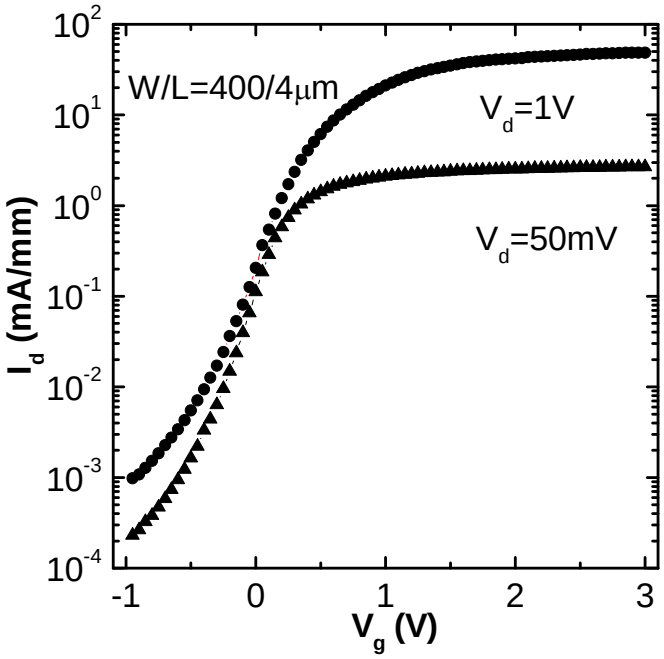


Fig. 2.20 : Log scale I_d-V_g of $In_{0.53}Ga_{0.47}As$ n-MOSFET of 4 μm gate length showing the subthreshold performance.

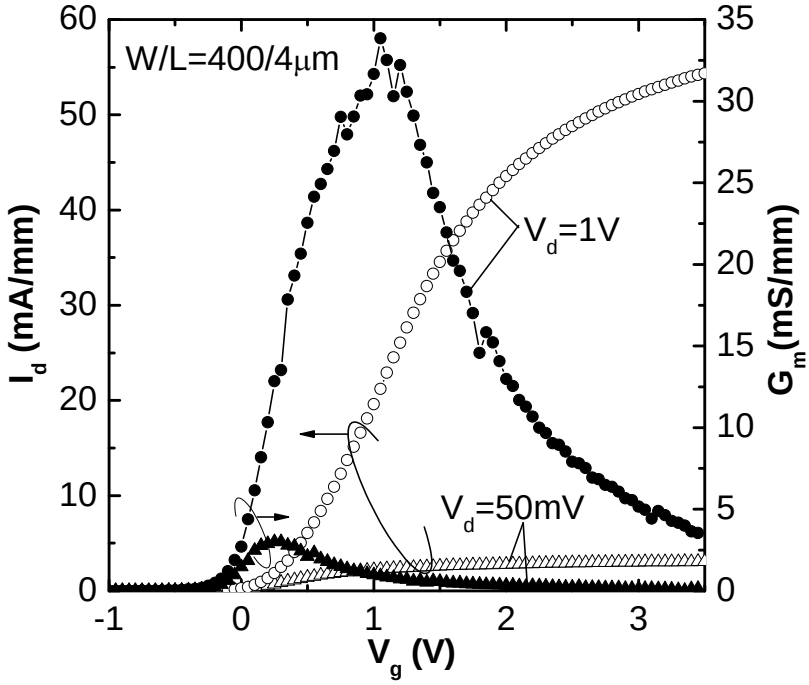


Fig. 2.21 : Linear scale I_d-V_g of $In_{0.53}Ga_{0.47}As$ n-MOSFET and gate transconductance versus gate bias with 50 mV and 1 V drain bias.

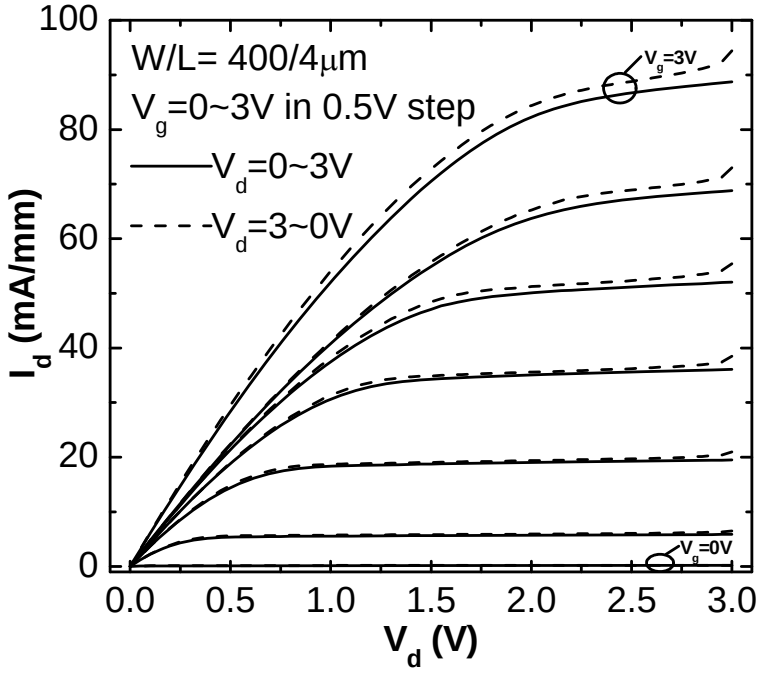


Fig. 2.22 : I_d-V_d of $In_{0.53}Ga_{0.47}As$ n-MOSFET of 4 μm gate length in a bidirectional drain bias sweeping for hysteresis study

2.7 Reference

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Chapter 3 : Interface Engineering of InGaAs MOSFET

3.1 Introduction

So far, the inversion-mode InGaAs MOSFET, with direct ALD or MOCVD deposited dielectric, demonstrated promising result. However, the interfacial quality between directly deposited high-k dielectric and III-V channel is still a concern, which is embodied in the large subthreshold swing [3.1]. Therefore, an innovative technique which further engineers the interfacial layer of the III-V MOS gate stack will be highly desirable. PH_3 passivation and Nitridation with thermal or plasma process have been used in group IV materials to engineering interfacial quality. Such passivation effect resulted in improved device performance in the Germanium channel MOSFET [3.3]. On the other hand, PH_3 passivation has been applied to GaAs MOS systems [3.4]. This concept can be applied to the InGaAs MOSFET fabrication [3.5].

On the other hand, HfAlO dielectric is a choice for thermal budget consideration in previous experiment. However, Al_2O_3 has a dielectric constant (k) of only 9, much less than the k value of HfO_2. The subsequent experiment also explores the use of HfO_2 as a dielectric for InGaAs MOSFET.

This chapter reports the comprehensive study of performance enhancement of InGaAs n-MOSFET by plasma PH_3 passivation. The calibrated plasma PH_3 passivation of the InGaAs surface before MOCVD high-k dielectric deposition significantly improves interfacial quality. X-ray Photoelectron Spectroscopy (XPS) studies confirm the suppression of Arsenic Oxide formation. By introducing plasma PH_3 passivation, the MOS capacitor with TaN/HfO_2/InGaAs gate stack is fabricated

and studied. Then by using the gate-first self-aligned process, the inversion-mode $In_{0.53}Ga_{0.47}As$ n-MOSFET is demonstrated with significant performance enhancement.

3.2 Process Integration

The InGaAs channel n-MOSFET in this study was fabricated by a process sequence described in Ref. [3.6], except for the CVD plasma PH_3 passivation. Starting substrate is the Molecular Beam Epitaxial (MBE) 500 nm strain-free $In_{0.53}Ga_{0.47}As$ on InP. The p-type dopant (Zinc) concentration in the vicinity of InGaAs surface is found to be $1x10^{17}$ cm^{-3} by the ECV method which was described in Chapter 2. After HCl and $(NH_4)_2S$ pre-gate cleaning, the InGaAs was loaded to the CVD chamber immediately and subjected to the plasma PH_3 passivation process at different conditions. The optimum condition was found to be 430 ^oC for 60 seconds with 300 sccm PH_3 mixed with N_2 with a ratio of 1:99. Some samples were then unloaded for X-ray Photoelectron Spectroscopy (XPS) study, while the rest were transferred to another chamber for high-k deposition without breaking vacuum. In this study, 10 nm MOCVD HfO_2 was deposited using $(Hf(OC(CH_3)_3)_4+O_2)$ as precursor, followed by the *in-situ* Post-Deposition Anneal (PDA) at 400 ^oC in N_2 ambient for 30 seconds. Reactive sputtered 150 nm TaN was subsequently deposited. The gate electrode was patterned by Chlorine gas based RIE. The samples were then divided into two sets: one for MOS capacitor study which is finished by back contact fabrication, another for continuing the MOSFET fabrication. The process followed the conventional self-alignment method, source and drain (S/D) was implanted with Silicon at 50 keV with dose of $1x10^{14}$ cm^{-2} and activated at 600 ^oC for 60 seconds by Rapid Thermal

Annealing (RTA). AuGe/Ni/Au and Ti/Pd/Au were deposited to form the front S/D contacts and the backside contact respectively.

3.3 Results and Discussion

3.3.1 Interface study

Cross-sectional transmission electron microscopy (TEM) images of a completed MOS capacitor structure are shown in Fig. 3.1. Fig. 3.1 (a) shows the control sample with direct HfO_2 deposition (without passivation) and Fig. 3.1 (b) shows the sample with plasma PH_3 passivation. High quality $TaN/HfO_2/InGaAs$ gate stacks are achieved where the conformal high-k films are observed in both TEM images. Electron Dispersion Spectroscopy (EDS) measurement was performed in the vicinity of the transistor channel region. Results show that out-diffusions of Oxygen and Hafnium to the channel are well-controlled. This is important for the achievement of high-quality gate dielectric interface and high electron mobility. There is a clear interfacial layer formed between the InGaAs and high-k dielectric by the PH_3 passivation and its thickness is about 1 nm.

Atomic Force Microscope (AFM) is used to examine the change in surface morphology due to passivation. InGaAs surface profiles after $HCl/(NH_4)_2S$ pre-gate cleaning shows RMS roughness of 0.68 nm in Fig. 3.2 (a). After plasma PH_3 passivation, its roughness is reduced to 0.31 nm in Fig. 3.2 (b). Inversion-mode MOSFET uses a surface channel, therefore, a smooth surface reduces interface scattering which degrades the carrier mobility in the channel at a high gate bias.

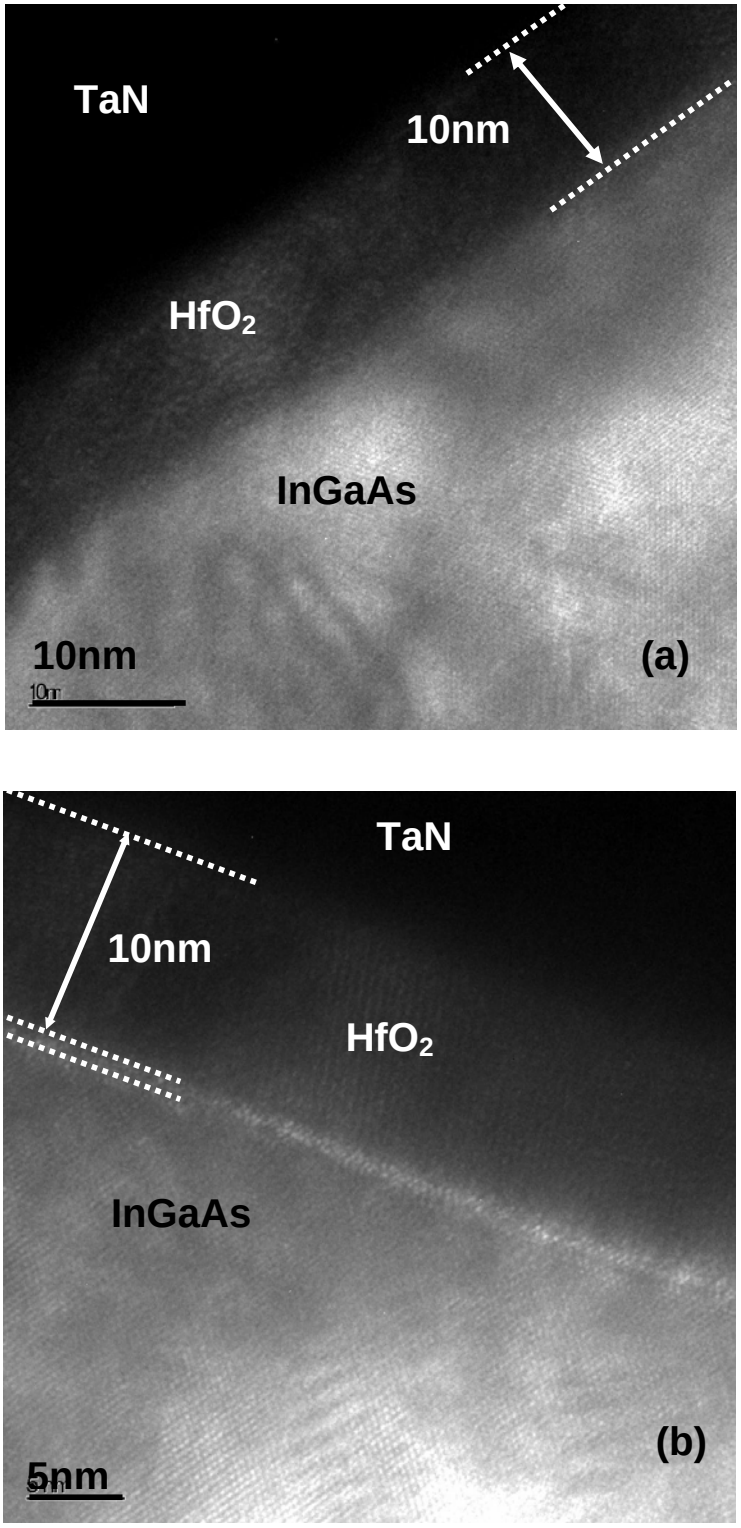

Fig. 3.1 : TEM images of the gate stacks by (a) HfO_2 direct deposition; (b) Plasma PH_3-passivation and HfO_2. Conformal high-k film, interface and substrate are seen for both cases. About 1 nm thick passivation layer is observed in plasma PH_3-passivation sample.

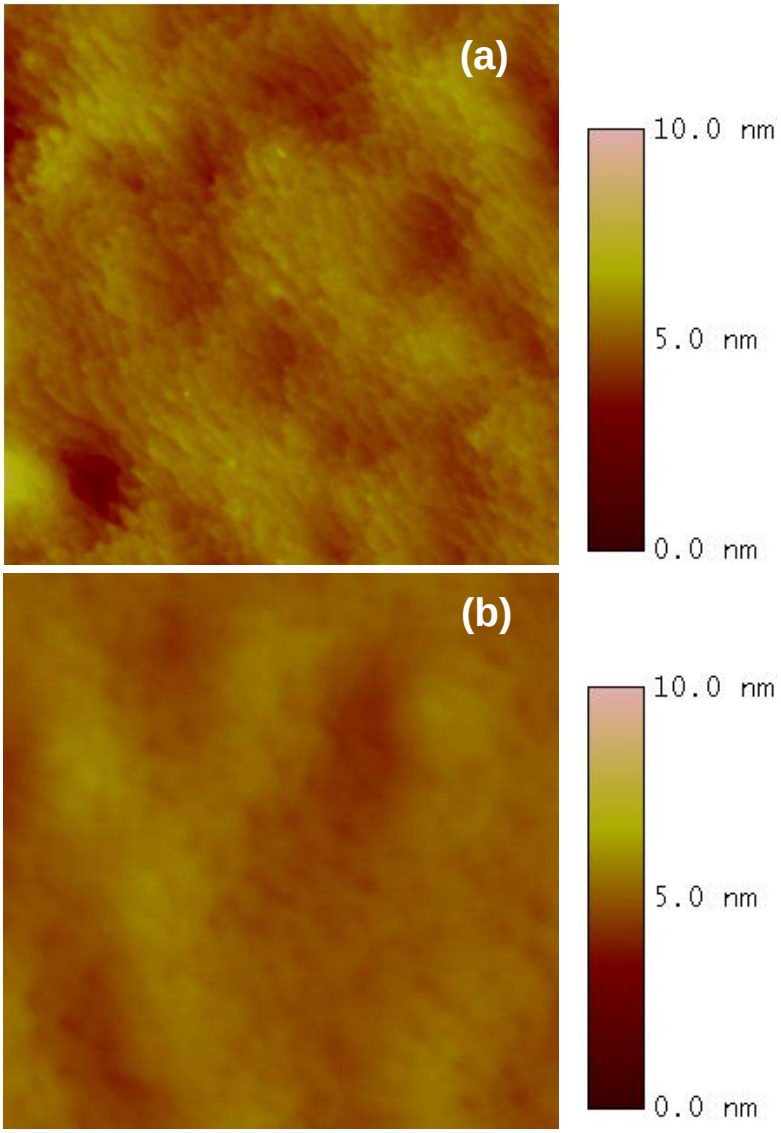

Fig. 3.2 : AFM image of the (a) InGaAs after pre-gate cleaning, (b) plasma PH_3-passivated InGaAs surface. The RMS roughness values for (a) and (b) are 0.682 nm and 0.312 nm, respectively. The scan windows are 5x5 μm^2.

XPS is used to study the element bonding on the surface after plasma PH_3 passivation. Phosphorus and Nitrogen are detected on the InGaAs surface as shown in Fig. 3.3 (S.C. = 0). The shallow incorporation and negligible in-diffusion of Phosphorus and Nitrogen on the passivated InGaAs surface are confirmed by the disappearance of P-2p and N-1s peaks after 5 Argon sputtering cycles (S.C.) which corresponds to a depth of about 2 nm.

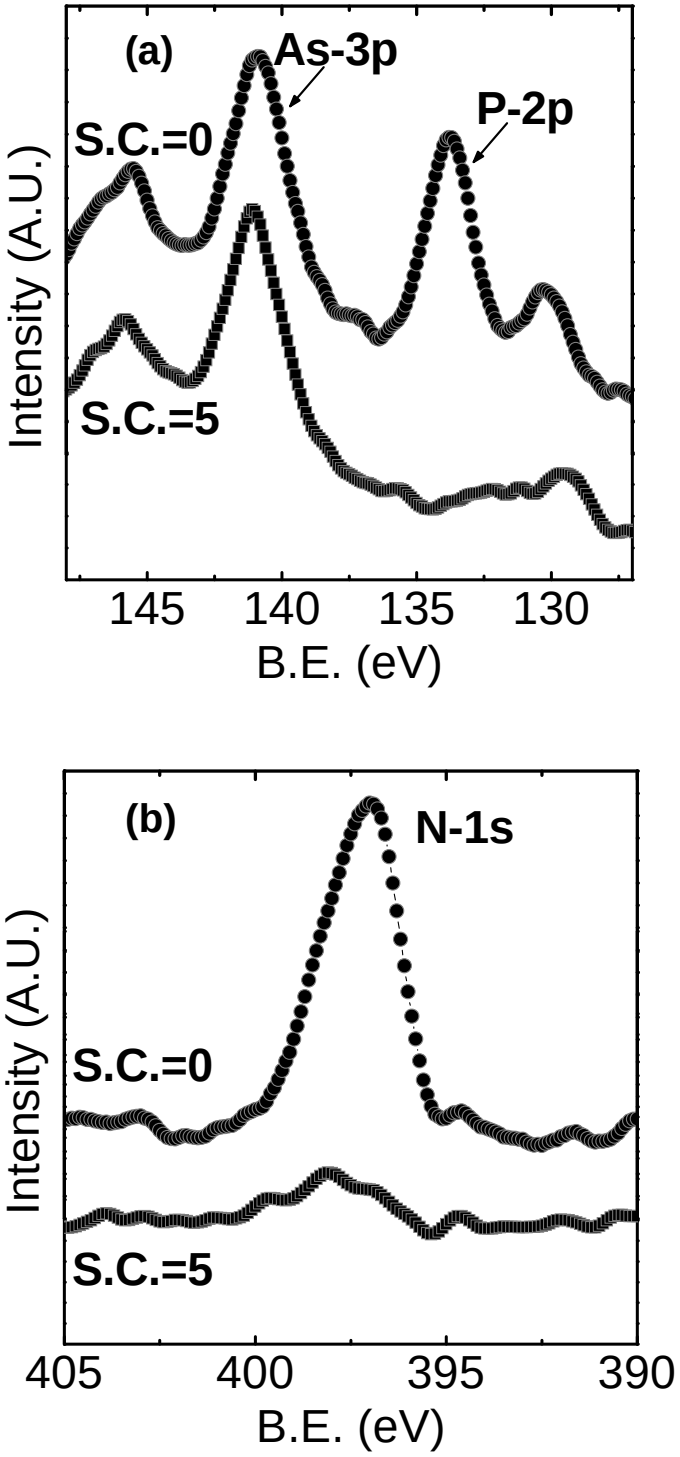

Fig. 3.3 : XPS study of the InGaAs surfaces plasma-PH_3-passivated sample detects the (a) P-2p peak and (b) N-1s peak. Both disappear after a sputtering of 5 cycles, equivalent to about 2 nm, confirming a very shallow surface incorporation of Phosphors with little in-diffusion. The P_xN_y forms a chemically stable compound which passivates the surface and smoothen the surface.

Arsenic Oxide is thermally unstable and is believed to introduce interface traps and degrade the MOS gate stack quality in following thermal processes. The Arsenic Oxide formation on InGaAs surface with and without passivation is studied by XPS. Fig. 3.4 shows the As-3d spectrum on both InGaAs surfaces after exposure to atmospheric ambient for similar and sufficiently long time. Fig. 3.4 (a) shows As-3d spectra for the sample that has undergone only pre-gate cleaning and Fig. 3.4 (b) is for the sample subjected to both pre-gate cleaning and plasma PH_3 passivation. In Fig. 3.4 (a), after decomposition, two peaks for Arsenic Oxide are found at binding energy of 44 eV and 45 eV, corresponding to As_2O_3 and As_2O_5 respectively. Among the two Oxide components found, As_2O_3 is the major Oxide component for the unpassivated sample. In Fig. 3.4 (b), no observable peak is found in the Arsenic Oxide binding energy. Thus it is observed that the Arsenic Oxide is formed on bare InGaAs surface while it is not detected on passivated InGaAs surface for the same time of atmospheric exposure. It is evident that plasma PH_3 passivation is more effective to suppress the Arsenic Oxide formation than the bare substrate. The previous chapter has found that, after merely pre-gate cleaning, InGaAs is less susceptible to Arsenic Oxide formation than GaAs by similar experiment but with a shorter exposure time [3.7]. This work shows that a passivated InGaAs results in further improvement with even better immunity to Arsenic Oxide formation. The interface trap densities (D_{it}) in the HfO_2/InGaAs gate stacks are extracted by the conductance method. Directly deposited and passivated samples have D_{it} of $4.3x10^{12}$ and $8.6x10^{11}$ $eV^{-1}cm^{-2}$ respectively. D_{it} is reduced in the passivated InGaAs/HfO_2 gate structure. Using different techniques to realize the Phosphorus passivation on InGaAs surface, *Pala* explained that there is a substitution of Phosphorus atoms for Arsenic atoms at the surface, with which Arsenic Oxide suppression is achieved and interfacial quality of

the MOS structure is improved [3.8]. We have recently found that, with our plasma PH_3 passivation process, the InGaAs surface is covered by a chemically stable P_xN_y layer which results from the PH_3:N_2 reaction. It accounts for the passivation effect and Arsenic Oxide suppression on InGaAs [3.9].

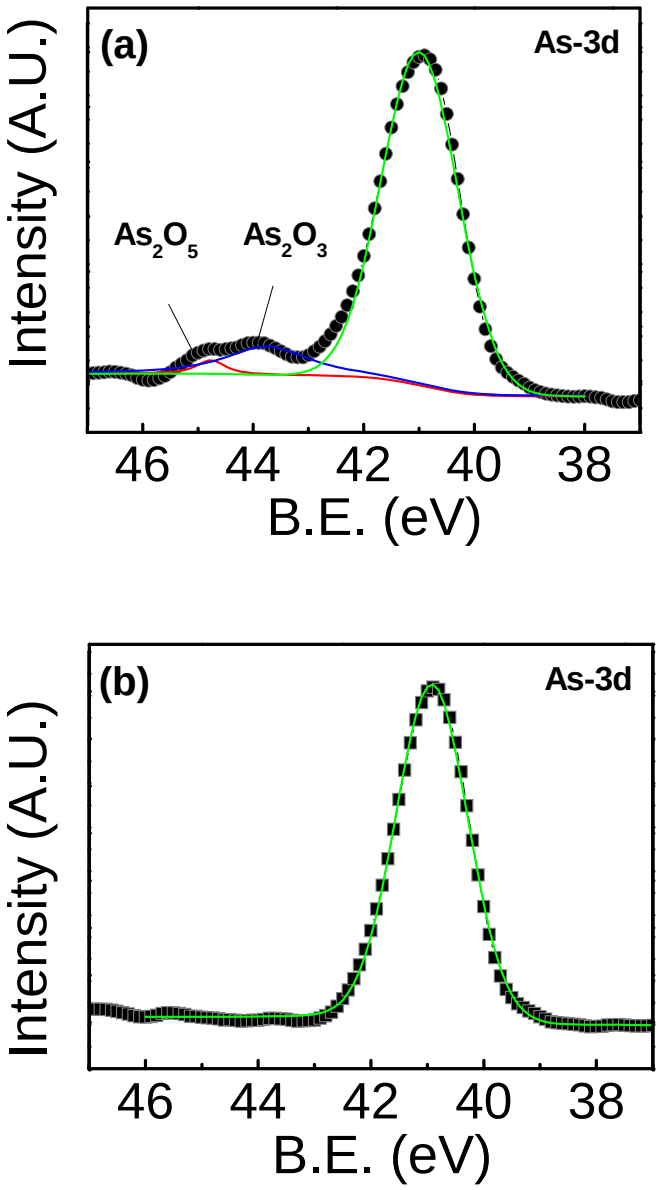

Fig. 3.4 : (a) As-3d peak on the non-passivated and (b) passivated InGaAs surface after exposed to atmospheric ambient for a sufficient long time. Thermally unstable Arsenic Oxide is found formed on unpassivated surface, while passivation suppresses its formation. In the first case, the decomposited Arsenic Oxide peak shows a major composition of As_2O_3.

3.3.2 Plasma PH_3 passivated InGaAs MOS capacitor

The Capacitance-Voltage (C-V) characteristic of the HfO_2/InGaAs MOS system with plasma PH_3 passivation is measured at 1 kHz in Fig. 3.5. The transition from depletion to accumulation agrees well with the simulated low frequency C-V characteristic considering quantum mechanical effect, indicating high quality gate stack. From the curve fitting, Effective Oxide Thickness (EOT) is extracted to be 3.0 nm and dielectric constant for the gate dielectric is 12.9. Flatband voltage is -0.5 V. Physical thickness for HfO_2 is 10 nm.

Capacitance from a HfAlO/InGaAs MOS system with plasma PH_3 passivation is shown in Fig. 3.6. Similar to that of HfO_2, the low frequency C-V agree well with the simulation curve in the transition region. An EOT of 1.7 nm is extracted from simulation curve. The flatband voltage is -0.62 V in this case. Physical thickness for HfAlO is 5.5 nm. To the author's best knowledge, the EOT 1.7 nm in this MOS capacitance system is one of the smallest in publications.

The gate leakage densities in directly-deposited and passivated HfO_2/InGaAs MOS system are measured and shown in Fig. 3.7. Similar leakage levels are observed for both cases. The EOT for both cases is 3 nm to 3.2 nm. The leakage density is around $1x10^{-5}$ A/cm^2 at gate biased of 2 V. The MOSFET gate leakage for directly deposited HfAlO on InGaAs has been reported in Fig. 2.15 of Chapter 2, which has 4.5 nm EOT and leakage of $1x10^{-6}$ A/cm^2 at V_g = 2 V. Considering the EOT of 3 nm, the leakage level is comparable with the recently reported TaN/HfO_2/GaAs MOS system as shown in Fig. 3.87 [3.5]. The low leakage level is attributed to the sufficient valence band offset (VBO) and conduction band offset (CBO). It is reported in Fig. 2.8 of Chapter 2, that directly deposited HfO_2 on InGaAs has VBO = 2.87 eV and CBO = 1.99 eV. The data is extracted by the VB spectra method.

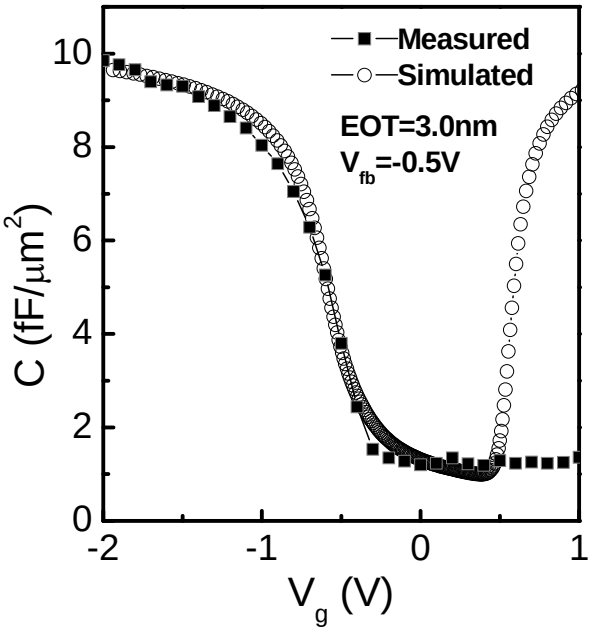

Fig. 3.5 : Capacitance-Voltage (C-V) characteristic at 1 kHz of plasma PH_3 passivated MOS capacitor with TaN/HfO_2/InGaAs gate stack. Simulation of ideal C-V characteristic is the Circled line. A close match between the simulated and measured curve indicates a high-quality MOS capacitor. Physical thickness for HfO_2 is 10 nm.

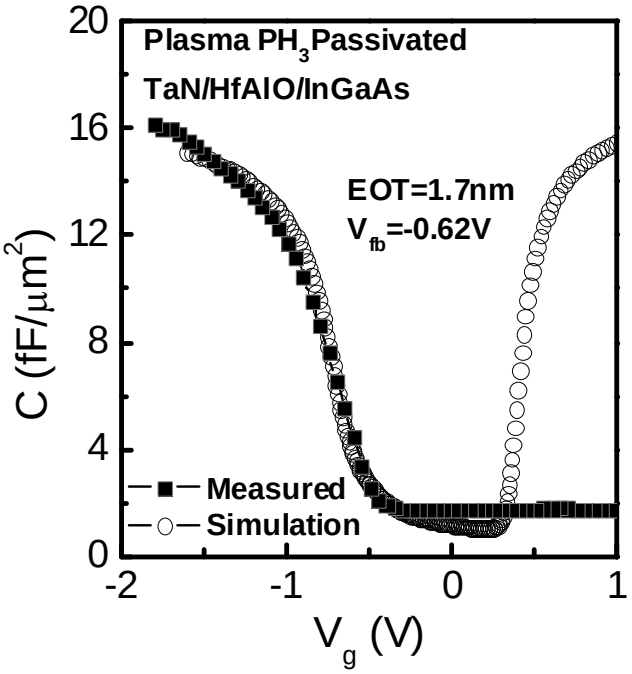

Fig. 3.6 : Capacitance-Voltage (C-V) characteristic at 1 kHz of plasma PH_3 passivated MOS capacitor with TaN/HfAlO/InGaAs gate stack. Simulation of ideal C-V with fitting parameters is the circled line. Physical thickness for HfAlO is 5.5 nm.

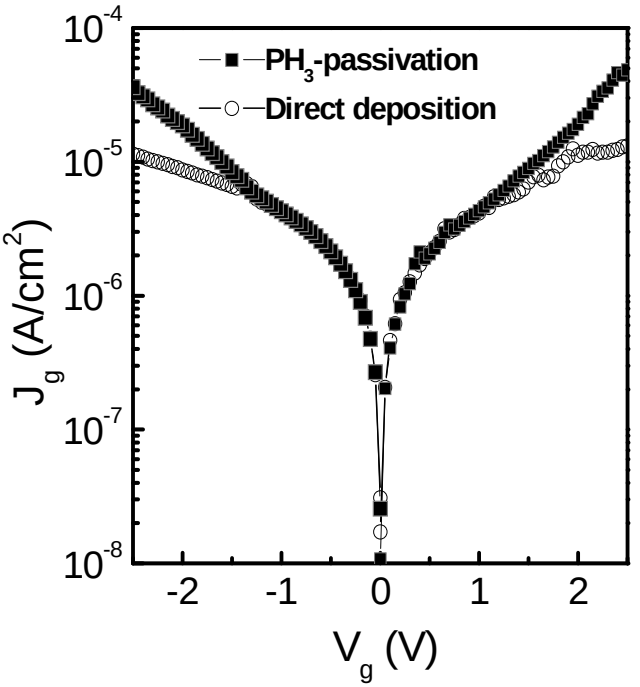

Fig. 3.7 : Gage leakage density of direct deposition (open circle) and passivated (solid rectangle) HfO_2/InGaAs MOS capacitors. Similar leakage levels are observed.

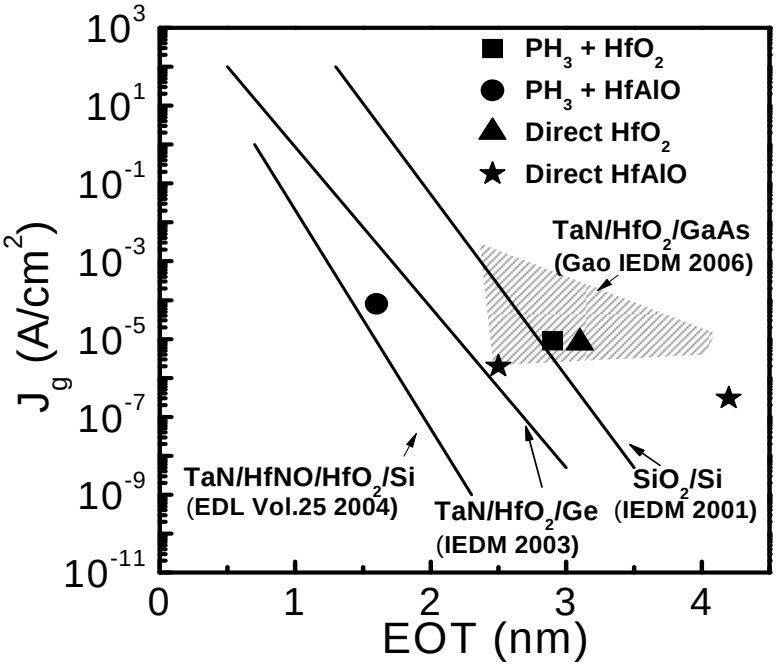

Fig. 3.8 : Gate leakage comparison with other MOS gate stack structures.

3.3.3 Plasma PH_3 passivated InGaAs MOSFET

The results in this section were measured from MOSFET that has S/D implantation and activation as well as S/D contact formation. Thus, the device has gone through the thermal process of 600 ^{o}C RTA.

By grounding the substrate and measuring the capacitance between gate and S/D (standard split C-V measurement for inversion capacitance), the C-V characteristic is measured from low frequency of 500 Hz to high frequency 1 MHz in Fig. 3.9. After the 600 ^{o}C annealing for S/D dopant activation, the MOS gate stack in the transistor shows stability. It exhibits very low frequency dispersion (< 5%) and small threshold voltage difference (< 0.1 V) from 500 Hz to 1 MHz. We attribute this excellent performance to the interfacial layer formed after passivation to prevent the substrate from oxidizing during the thermal treatment and to reduce the interface state density. Bi-directional C-V measurement is done at 10 KHz, sweep rate of 160 mV/s and sweep range from −0.5 to 2 V. Measured hysteresis is 0.17 V as shown in Fig.3.10. As discussed in our previous MOS capacitor study on InGaAs and GaAs, high Indium concentration at the interface effectively improves trapping charge behavior of the dielectric, and thus the hysteresis. A reduction of hysteresis from 2 V in p-GaAs MOS capacitor to 0.5 V in p-InGaAs MOS capacitor is observed with HfAlO (HfO_2:Al_2O_3 = 9:1) dielectric [3.7]. The passivation in this work further improves hysteresis, so better quality of bulk trap in the dielectric and interface trap are expected.

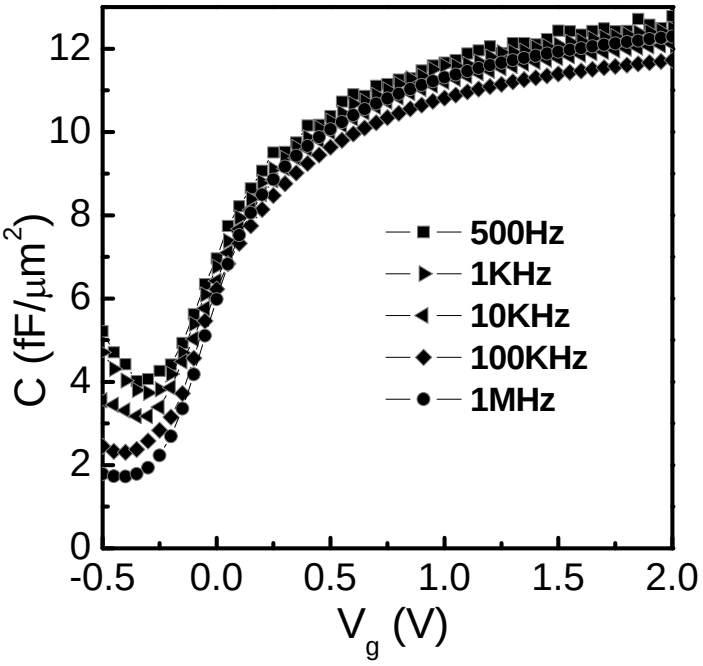

Fig. 3.9 : Plasma PH_3 passivated MOSFET inversion capacitance versus applied gate bias from 500 Hz to 1 MHz. It has low frequency dispersion, indicating low interface traps in a wide range of frequencies and successful channel formation.

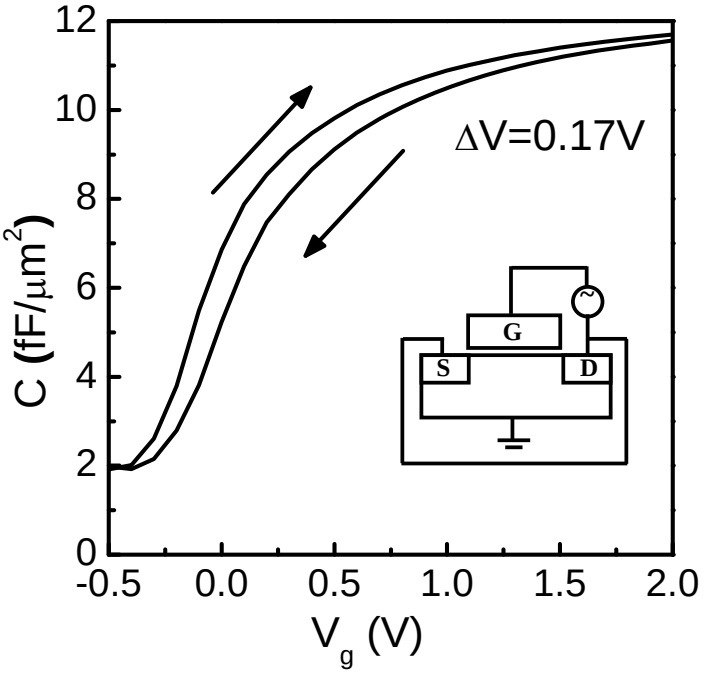

Fig. 3.10 : The hysteresis of inversion capacitance at 10 KHz from -0.5 V to 2 V measuring range. Inversion capacitance measures between gate to source and drain with substrate grounded, shown in the inset.

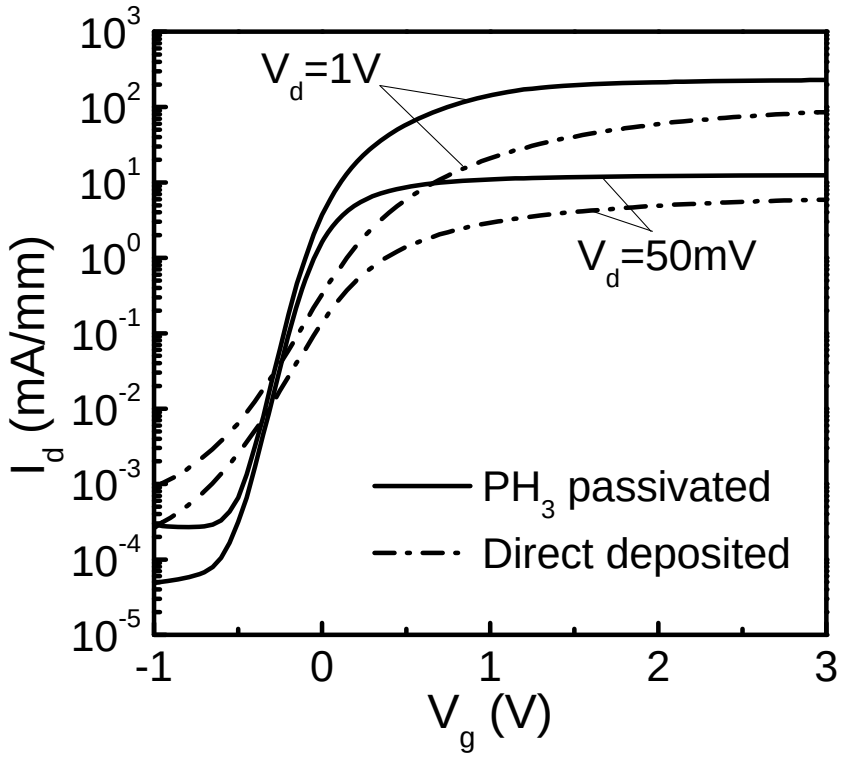

Fig. 3.11 : Drain current at the subthreshold region. Log scale I_d-V_g of InGaAs n-MOSFET of 4 μm gate length with 50 mV and 1 V drain bias for passivated MOSFET (solid) and directly deposited control (dash-dot).

Fig. 3.11 shows the I_d-V_g characteristics for the directly deposited and passivated InGaAs n-MOSFET of 4 μm gate length. By using plasma PH_3 passivation, the mean subthreshold swing (S.S.) is 100 mV/dec, I_{on}/I_{off} ratio is 5 orders to 6 orders, drain induced barrier lowering (DIBL) is 92 to 18 mV/V. From the recently reported inversion-mode InGaAs n-MOSFET, S.S. is usually above 200 mV/dec at room temperature and increases rapidly at elevated temperature [3.1]. For the reported GaAs and InGaAs n-MOSFET with Silicon interface passivation layer (IPL), S.S. is above 120 mV/dec [3.10]. Such poor performance in the S.S. may indicate the existence of significant interface traps.

Fig. 3.12 shows the I_d-V_d characteristic of InGaAs MOSFET of gate length 4 μm. Well behaved output characteristic is shown. At maximum bias condition (V_g = V_d =

3 V), 400 mA/mm drain current is obtained. There is a four-time increase in the on-state current for passivated samples over the directly deposited control samples.

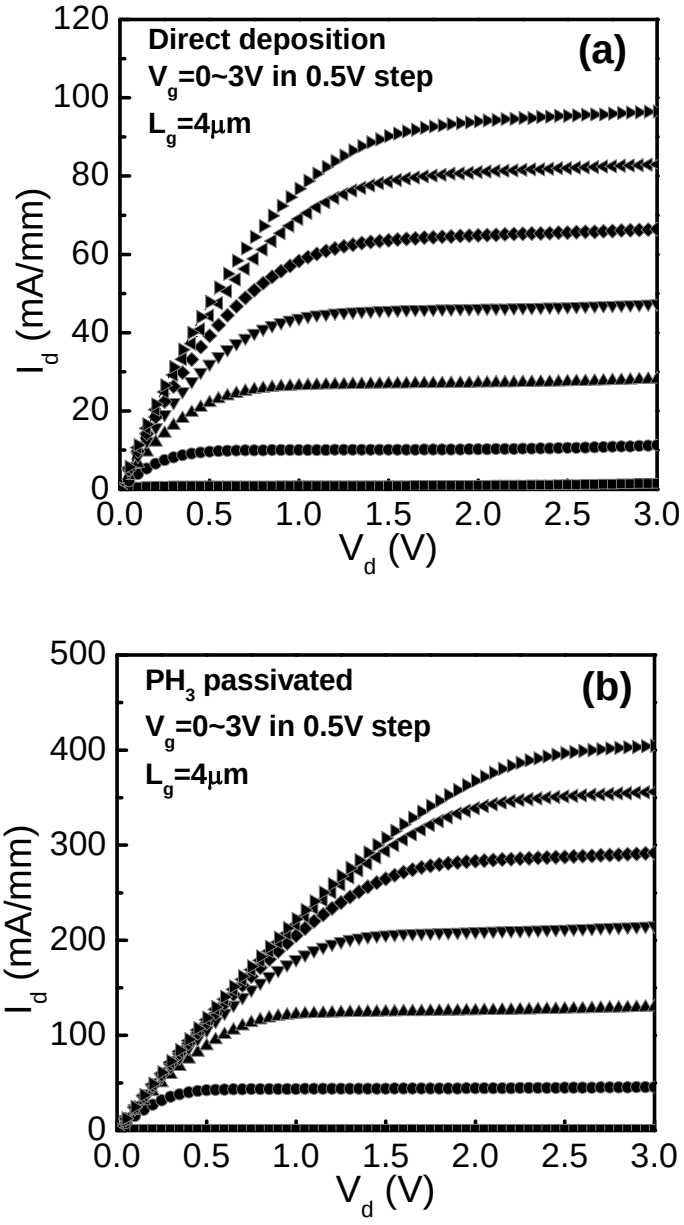

Fig. 3.12 : I_d-V_d of HfO_2/InGaAs MOSFET for (a) without (b) with PH_3-passivation.

The linear I_d-V_g characteristic and corresponding transconductance are shown in Fig. 3.13 for the passivated transistor under drain bias of 0.05 V and 1 V. The gate length is 4 μm. The maximum transconductance is 20 mS/mm and 180 mS/mm for

the two drain biases respectively. The threshold voltages are ~ 0 V. The workfunction is related to the effective metal workfunction, channel doping and Fermi-level pinning in the gate stacks. With a modulation of work function of gate electrode, the threshold voltage can be changed to fulfill the enhancement-mode n-MOSFET operation. The effective gate workfunction tuning for TaN and high-k dielectric has been reported in Silicon n-MOSFET [3.11]. The decrease in transconductance at high gate bias (V_g > 1.6 V) is due to the S/D series resistance. S/D series resistance is about 2.1 Ω.mm. This value is about half of the total resistance ($R_{channel}$ and R_{sd}) at V_g = 1.6 V. It becomes a limiting factor for the continuous current increase. Therefore, the reduction of S/D series resistance is imperative for further exploration of InGaAs n-MOSFET. In Fig. 3.14, the drain current hysteresis is shown. A threshold voltage shift of 55 mV is observed from a sweeping range of -1 V to 1.5 V at V_d = 1 V. It indicates the dielectric has a high quality and immune to bulk and interface trappings.

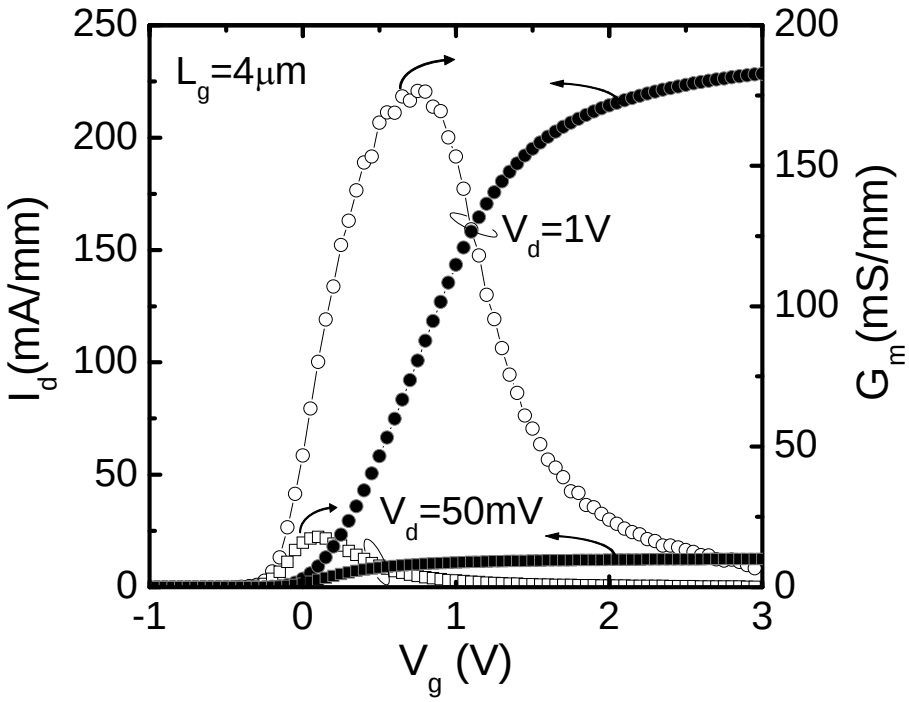

Fig. 3.13 : I_d-V_g characteristics and corresponding transconductances for passivated InGaAs n-MOSFET with 4 μm gate length at drain bias of 0.05 V and 1 V.

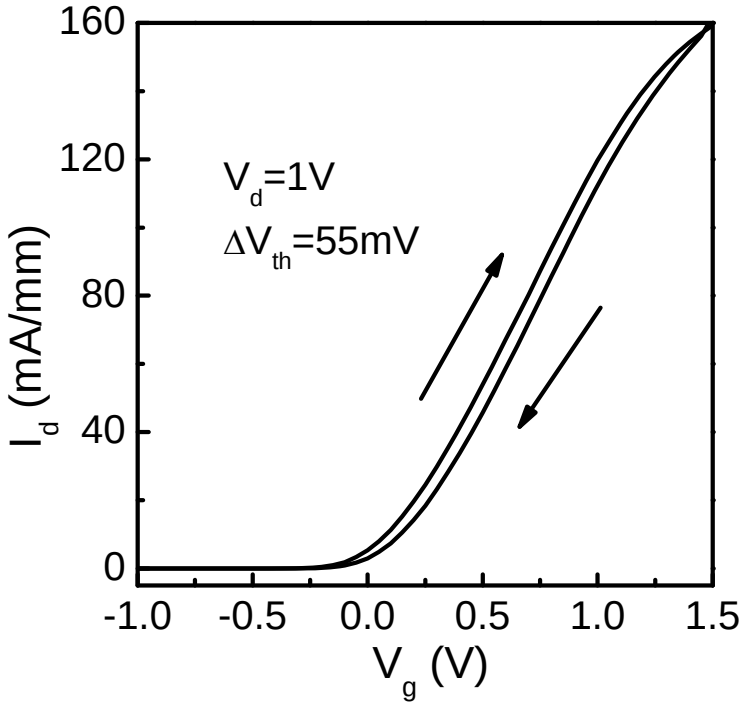

Fig. 3.14 : Drain current hysteresis for a bi-directional sweeping of gate voltage from -1 V to 1.5 V at drain bias of 1 V.

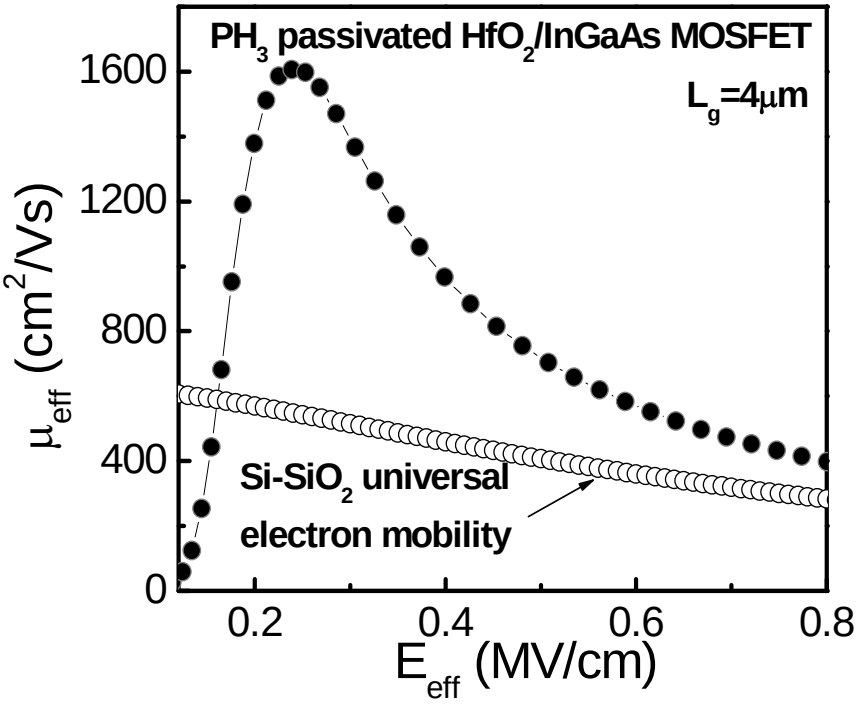

Fig. 3.15 : Channel electron mobility versus effective electric field extracted from an InGaAs n-MOSFET of 4 μm gate length by the split C-V method.

The electron mobility in the channel is extracted by the split C-V method without considering D_{it} and series resistance as shown in Fig. 3.15. Result shows that the peak mobility reaches 1600 cm^2/Vs. As in a conventional MOSFET, the low field mobility is restricted by Coulomb scattering which strongly depends on the impurity doping in the channel. Further research in advanced device engineering to minimize the impurity scattering effect can be promising to fully explore the benefit of the low effective mass of electrons in InGaAs.

3.3.4 Comparison with other III-V MOS systems

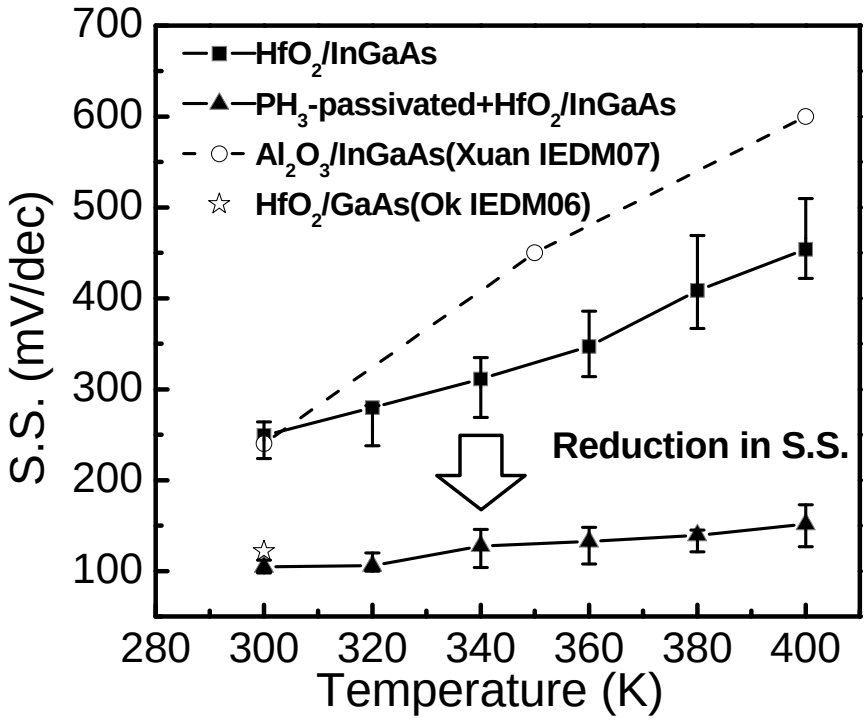

Fig. 3.16 : The subthreshold swing comparison of passivated InGaAs n-MOSFET (triangle) with direct deposition (square) over a temperature from 300 K to 400 K. The scale bars indicate the maximum and minimum S.S. values and solid symbols indicate the mean value of all measured devices.

Fig. 3.16 shows the S.S. of passivated and non-passivated MOSFET at various temperatures. The comparison shows that the plasma PH_3 passivation results in significant reduction of S.S. and its variation. As temperature rises, the increase in S.S. of the passivated MOSFET is less than directly deposited ones. To the author's best knowledge, the lowest S.S. of 96 mV/dec at room temperature (300 ^oC) for plasma PH_3 passivated MOSFET in this work exhibits a record value for inversion-mode III-V MOSFETs.

Fig. 3.17 compares the on-state current at $V_g = 2$ V and $V_d = 1$ V for the passivated n-MOSFET and directly deposited control. Significant increase of drain current from passivation is observed in the plot of on-state current versus various gate lengths.

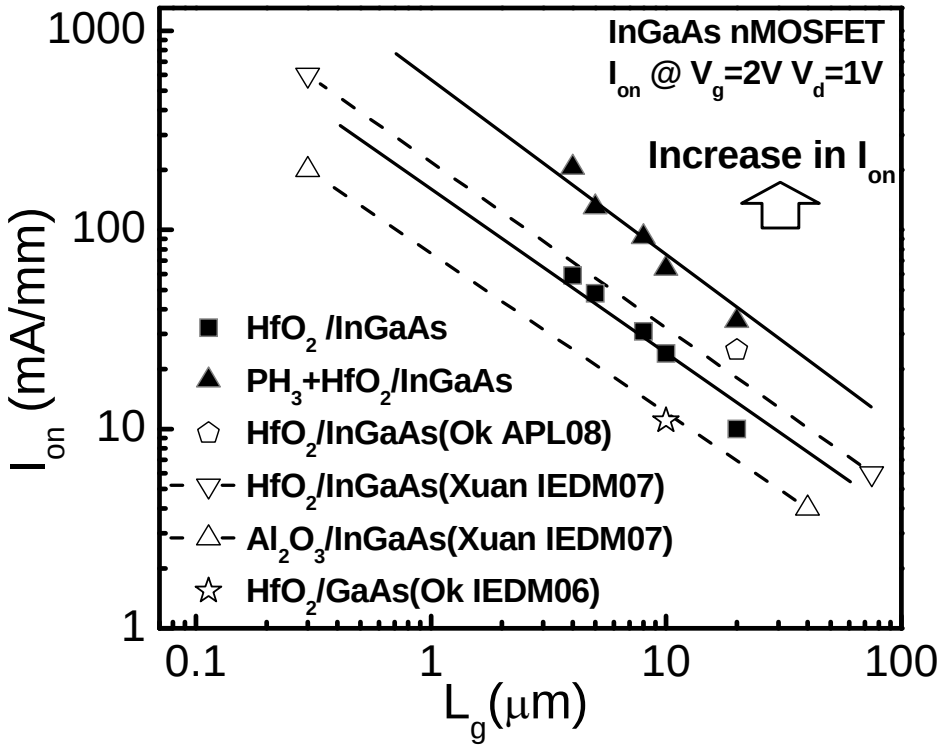

Fig. 3.17 : On-current versus gate length comparison under similar gate overdrive in n-MOSFET with passivated and directly deposited InGaAs n-MOSFET. A significant

increase in drive current is obtained with the interface engineering on HfO_2/InGaAs gate stack.

3.4 Summary

In this chapter, a novel interface engineering scheme is integrated into the fabrication of inversion-mode InGaAs MOSFET. A calibrated plasma PH_3 treatment has been shown to improve the interfacial quality by suppressing the interfacial oxide formation and interfacial state in the HfO_2/InGaAs gate stack. It also reduces InGaAs surface roughness. The MOS capacitor shows a similar leakage level for passivated and non-passivated samples. The C-V measurements on a MOSFET show low frequency dispersion and well behaved inversion channel formation. Subthreshold swing, transconductance and drive current have significant improvement with the plasma PH_3 passivation. Peak electron mobility of 1600 cm^2/Vs is reported.

3.5 Reference

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Chapter 4 : Scaling of InGaAs MOSFET

4.1 Introduction

The researches on IC device are always driven with the goal of small device footprint, high circuit density and small intrinsic delay. As introduced in Chapter 1, the III-V channel transistor is one promising candidate for future sub 32 nm technology node. From the ITRS roadmap projection, the physical gate length for 32 nm technology node is expected to be smaller than 15 nm.

So far, the III-V MOSFET in this work has a gate length in μm scale. In order to study the carrier transport, and eventually compare the figure of merits with Silicon for the same technology node, continuous scaling and novel structure for III-V MOSFET are imperative. Currently III-V channel transistors appeared in literature do not serves this purpose very effectively. The HEMT can strive for a very small gate length. The gate length has been shrunk to 30 nm range in recent publication [4.1]. However, the HEMT device usually requires a large footprint. The gate electrostatic coupling and gate leakage is an unsolvable trade-off. On the other hand, for InGaAs MOSFET, the dielectric last and gate last process used in its fabrication suffers from alignment problem. This result in tremendous difficulties in scaling the device dimension. Considering the fabrication flow, it is difficult to make smaller gate length exactly aligned with the removed dummy gate and implanted region [4.2].

From the process integration in Chapters 2 and 3, one key innovation in this work that has not been applied to previous InGaAs MOSFET is the self-alignment process. Self-alignment has long been used in Silicon MOSFET fabrication. It is a critical step with which the device in VLSI circuit can reach its present small dimension. Traditional CMOS process emphasizes self-alignment in LDD implantation, spacer

formation, S/D implantation, Silicide formation. In this work, implantation alignment is mainly defined for implantation.

To pattern small line widths, the conventional optical lithography system, i.e. mask aligner, is not a suitable tool because the optical technique could not easily achieve sub half μm pattern without complicated immersion or UV system. Thus, electron beam lithography (EBL) is used in this study. PMMA resist of a resolution better than 0.1 μm is used for EBL. A 950k molecular weight PMMA resists are selected for this work.

PMMA is good for high resolution lithography, but it is a poor mask material for etching [4.3]. One engineering challenge for using EBL is that, unlike the optical photoresist (such as AZ5214), the PMMA resist cannot sustain the plasma RIE during TaN pattern transfer. To overcome this problem, a hard mask has to be used for RIE.

This study starts from finding a suitable hard mask material to define small gate feature by etching the TaN. Demonstration of conformal feature down to 40 nm is shown. Then the series resistance and junction study is followed. First process flow is carried out with successfully device demonstration. By identifying the drawback of the first process flow, another modified approach is introduced. The series resistance effect is further investigated, which turns out to be the main drawback to further study. A device of 600 nm gate length shows current above 800 mA/mm.

4.2 Nano-sized Structure

4.2.1 Process design

The pattern transfer process is shown in Fig. 4.1. Firstly, the normal MOS structure is fabricated as described in Chapter 2 and as in Fig. 4.1 (step a). Secondly,

PMMA is spin coated onto the TaN surface (step b). The wafer is then loaded to the EBL chamber. Arbitrary pattern features on nanometer scale can be easily achieved by using AutoCAD software to design the EBL track (step c). Then a thin layer of metal hard mask is deposited onto PMMA (step d), followed by the lift-off process (step e). The RIE is then used to etch the TaN where there is no hard mask protection (step f).

4.2.2 Selection of hard mask material

The criteria for the hard mask include the following. Firstly, it should be resistive against RIE etching. Secondly, the pattern transfer after lift-off and etching should be faithful to the EBL drawing. Thirdly, its adhesion on TaN should be good. Considering the first criterion, inert metals are good candidates and chosen as the gate mask. Having high workfunction and chemically non-reactive, they do not easily form volatile by-products when subjected to the RIE. For the second and third criteria, experiments are carried out by using Ni (10 nm and 50 nm) and Pt (10 nm).

Fig. 4.2 shows the SEM images after RIE by using 10 nm Ni as hard mask. The resultant pattern is not smooth at the edge of the line at higher magnification. Fig. 4.3 (a) shows the SEM image patterned by using 50 nm Ni as hard mask. The pattern is straight but there is some shadow at the edge. By further investigation with AFM, it is identified that around the edge, there are un-removed material of step height which is 20% higher than the original height in Fig. 4.3 (b and c). This can be the non-volatile residual from Ni compound by-product. It may also be due to the thicker Ni layer form T-shape pattern after lift off. The “eave” of the T-shape Ni shadow RIE to a certain extent.

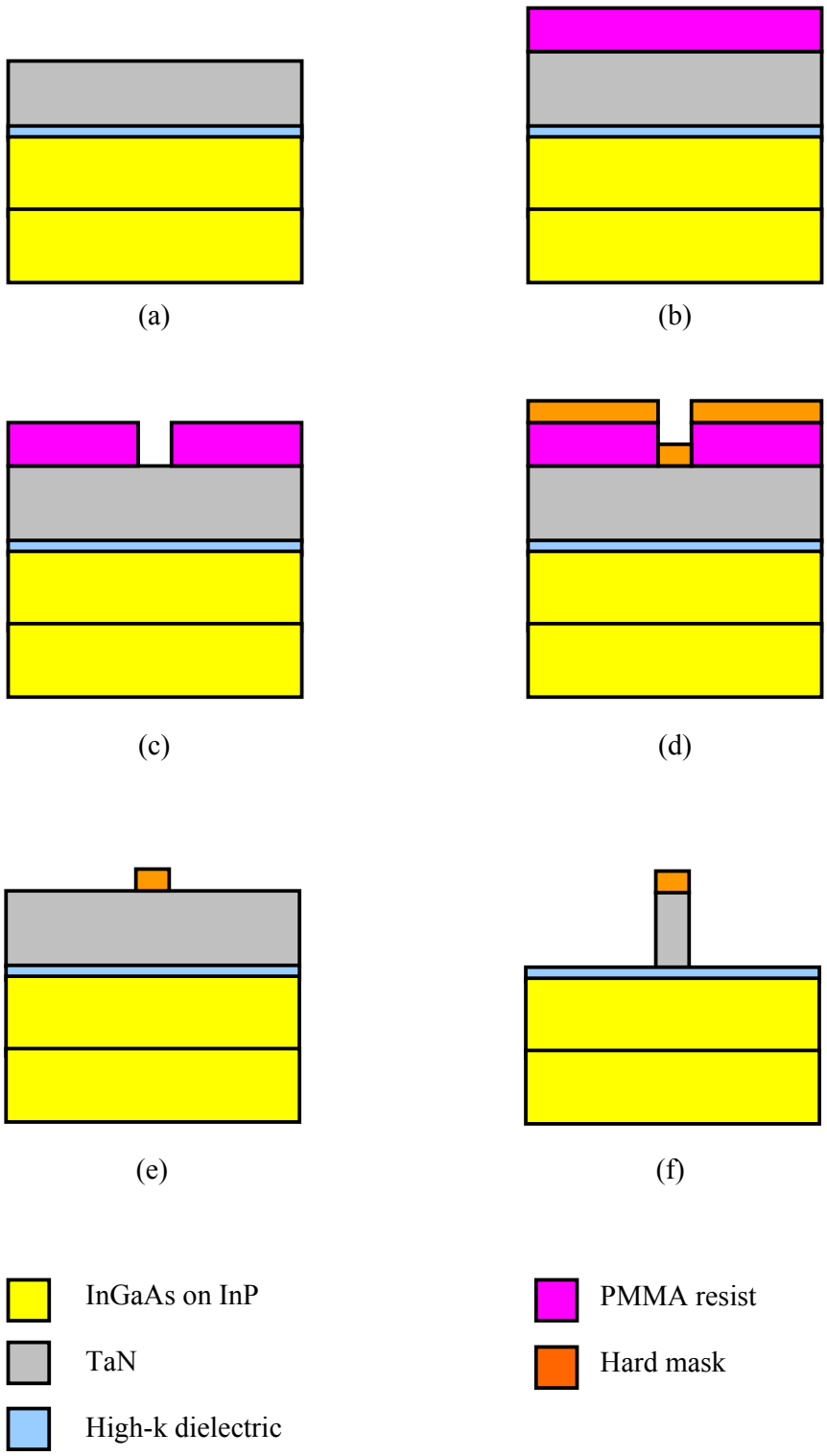


Fig. 4.1 : Fabrication of gate feature of very fine line width. (a) Gate stack (b) Spin coat of PMMA resist (c) EBL drawing and developed pattern (d) Hard mask deposition by E-beam evaporation (e) Lift off (f) RIE etching.

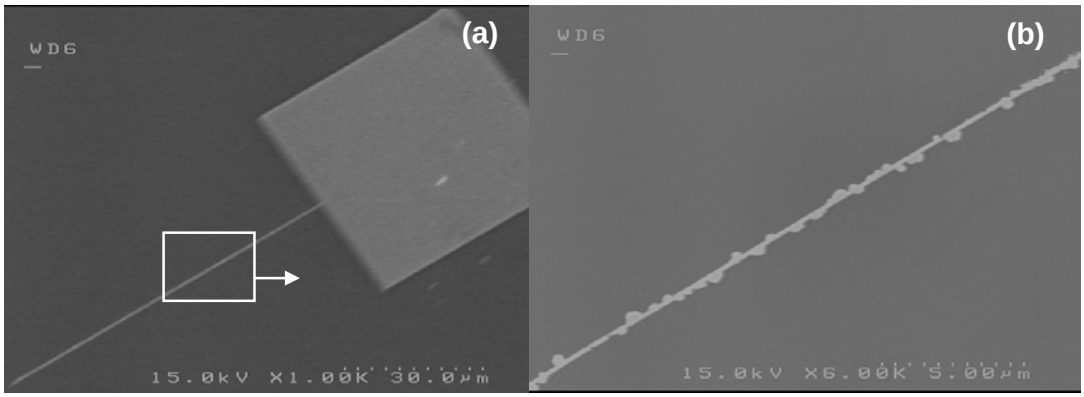


Fig. 4.2 : SEM images after RIE etching of TaN using 10 nm thickness Ni as hard mask. (a) low magnification image (b) high magnification image. The line is not straight.

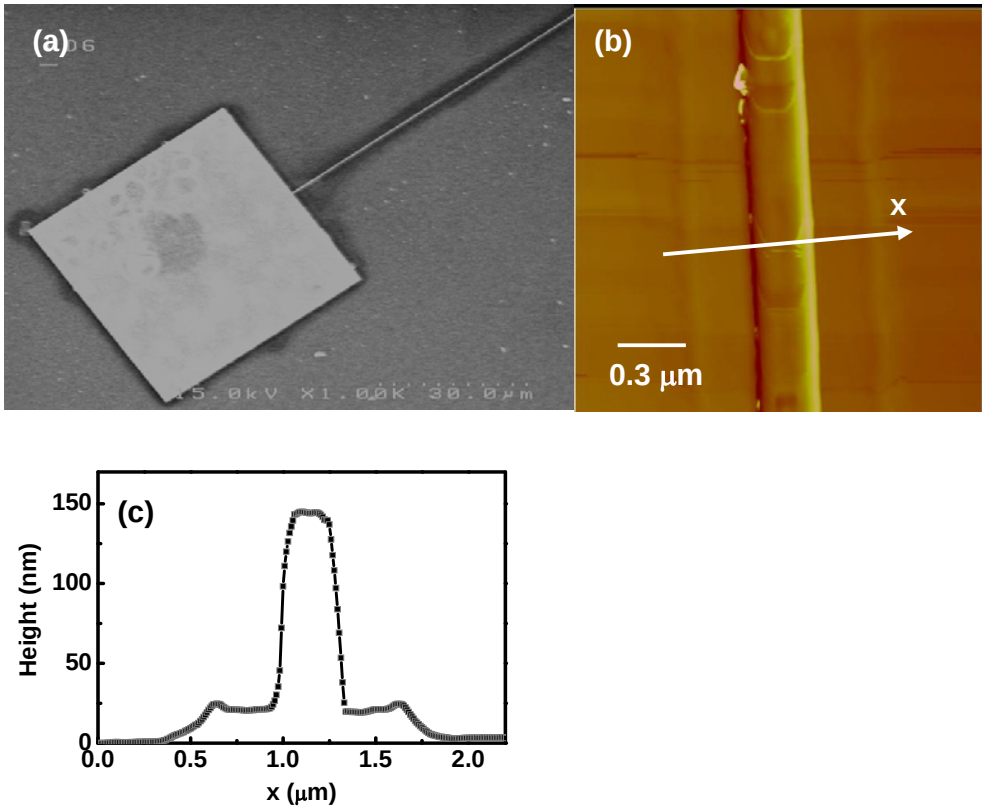


Fig. 4.3 : 50 nm thickness Ni as hard mask after RIE etching. (a) low magnification SEM image. A shadow is shown at the edge of the pattern. (b) AFM image of 2x2 μm^2 window. (c) Surface profile height versus distance *x* across the line in image (b). The shadow areas are the non-removed material.

Fig. 4.4 shows the SEM image using 10 nm Pt as hard mask. It is observed that the EBL drawn pattern is well preserved after etching. The edge is smooth and the

line width is 128 nm. A further AFM investigation is carried out. The smooth edge is confirmed and the bottom corner is sharp with no residual step. Note that the line width from the SEM and AFM is not exactly the same. Considering the aspect ratio and small line width features of the sample, the AFM measurement may be interfered by the sharpness of its tip. Nevertheless, it is concluded that Pt is the material of choice for subsequence short channel fabrication.

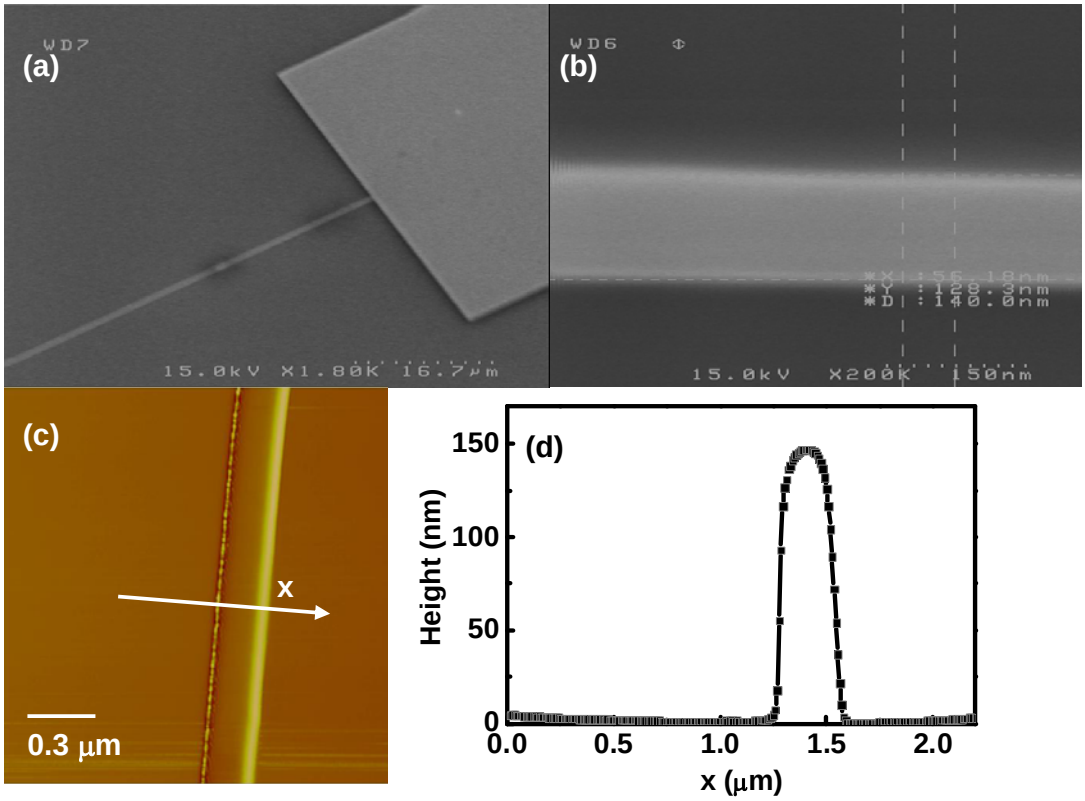


Fig. 4.4 : 10 nm thickness Pt as hard mask after RIE etching. (a) low magnification SEM image. (b) high magnification SEM image shows the line width is 128 nm. (c) AFM image of 2x2 μm^2 window. (d) Surface profile height versus distance *x* across the line in image (c). Clear and straight line is observed.

4.2.3 Pattern transfer

Cross section TEM images are taken from the fabricated device structure. A uniform and conformal line is observed in the pattern transfer onto TaN after RIE. It

is clearly observed, that the thickness of TaN is about 100 nm and Pt is about 10 nm. The Pt is not attacked by the RIE process. The sidewall of TaN is straight and sharp. There is no residual TaN or by-product seen by the image. The line width of 49 nm and 40 nm are successfully obtained.

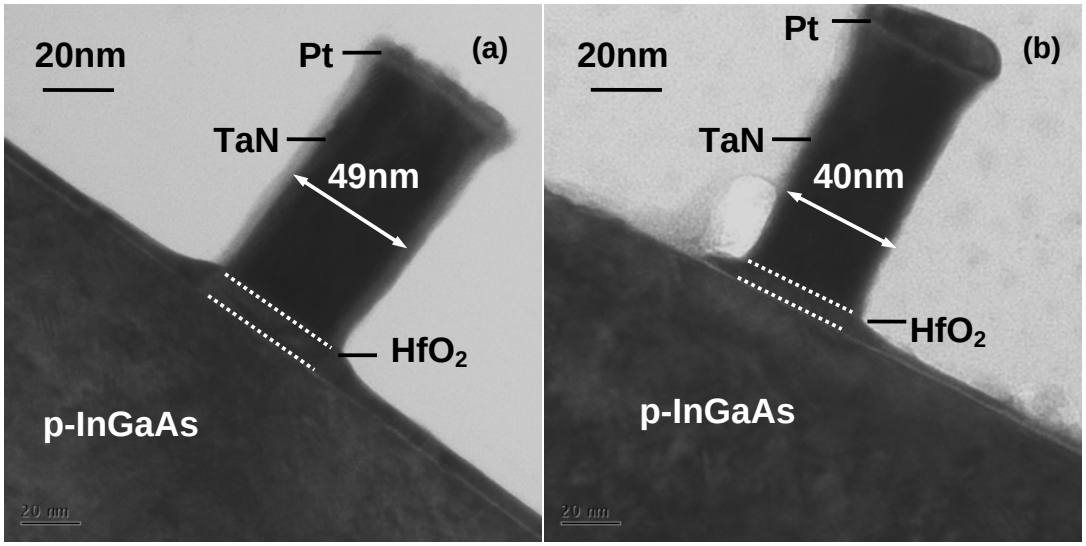


Fig. 4.5 : 10 nm Pt hard mask is used to fabricate MOS structure. The TEM cross section of gate length of 49 nm and 40 nm are shown in (a) and (b) respectively. Straight edge with aspect ratio of 2.5:1 is obtained.

4.3 Source and Drain Consideration

To have better short channel performance, the junction depth should be scaled along with the source and drain spacing. A Monte Carlo simulation is carried out using Tsuprem®. Silicon is implanted through a 10 nm SiO_2 into InGaAs. The dopant distribution as a function of depth from the surface is shown in Fig. 4.6. Implantation energy of Silicon is from 10 keV to 100 keV. Ignoring the 10 nm SiO_2, the distribution of 100 keV Silicon profile is similar to the measured dopant profile in the as-implantation sample by energy 100 keV and dose 4.1×10^{13} cm^{-2} [4.4], implying a

match of simulation with experiment. From the MC simulation, Energy of 20 KeV is chosen to control the implantation depth around 75 nm.

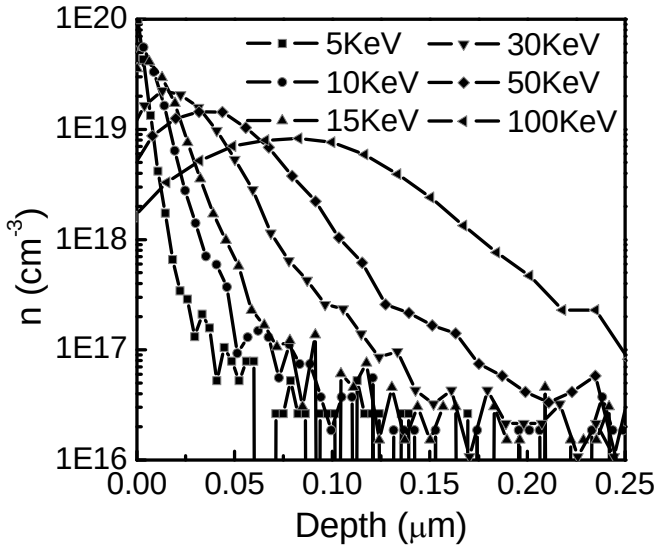


Fig. 4.6 : MC simulation of as implanted dopant distribution profile as a function of depth. Implant dose is $1x10^{14}$ cm^{-2}.

The trade-off of using a reduced junction depth is the increased in source and drain series resistance. In this case, the sheet resistance portion of the S/D series resistance turns out to be the major issue. In fact the same problem has been discussed in Chapter 3. When a high current is running through the device channel, the series resistances play a more vital role in limiting the current than the gate resistance, thus the transconductance.

4.4 Process Integration

The process integration to make a sub μm scale channel length MOSFET is shown in Fig. 4.7. The process is originated from the self-aligned fabrication previously shown in Fig. 2.13. The yellow bullet highlights the procedures which are different from the long channel device fabrication, which includes using Electron Beam

Lithography (EBL) and hard mask instead of photolithography to pattern the gate, and using another EBL to draw the S/D contact opening area instead of photolithography.

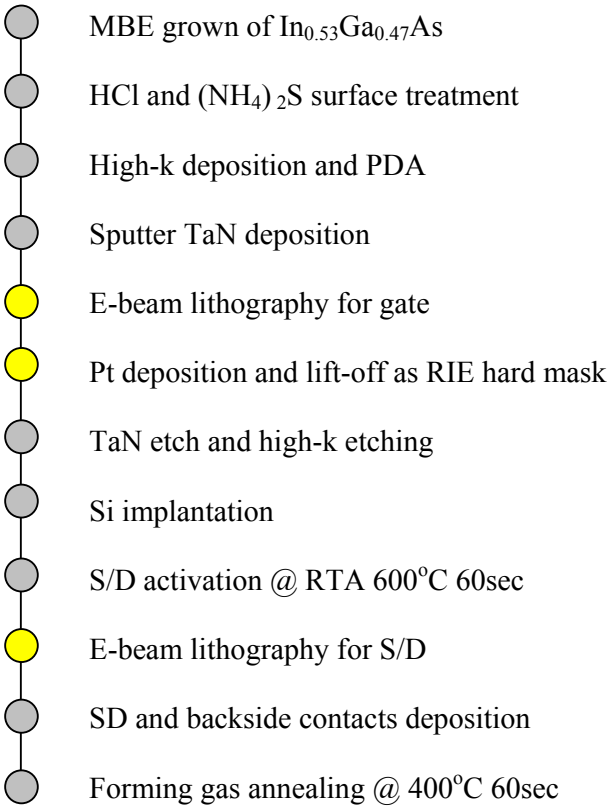


Fig. 4.7 : Process integration of short channel InGaAs MOSFET. Yellow bullet indicates the step different from long channel transistor fabrication.

Using the self-aligned gate-first process, sub 100 nm HfO_2/InGaAs MOSFET is fabricated without PH_3 passivation. Pt is used as mask material, resistive to the RIE etching. TEM cross section of the fabricated device is shown in Fig. 4.8 where the TaN gate length is 95 nm. Fig. 4.9 shows the output performance of I_d-V_g and I_d-V_d. DIBL is 105 mV/V and S.S. is 164 mV/dec. Due to the long distance between S/D contacts and a relatively shallow implantation, parasitic series S/D resistance is one major source for on-current degradation. Estimated S/D resistance is as high as 2.1 Ω.mm. In additional, the less satisfactory interface from direct deposition should be

addressed to account for on-current degradation. Advance surface engineering of PH_3-passivation and process optimization is believed to be imperative for further analysis.

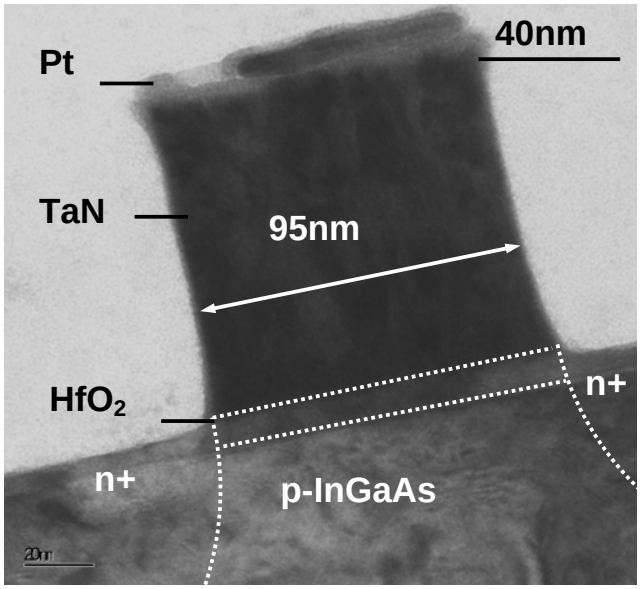


Fig. 4.8 : TEM image of cross section of InGaAs MOSFET with directly-deposited HfO_2 gate dielectric, Pt hard mask defined 95 nm TaN gate, self-aligned S/D implantation.

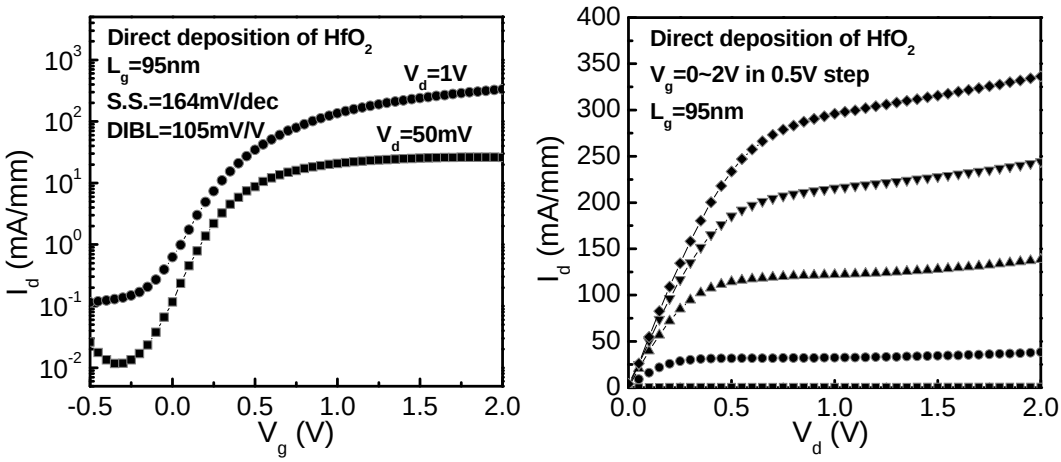


Fig. 4.9. I_d-V_g and I_d-V_d characteristics of 95 nm gate length InGaAs MOSFET directly-deposited HfO_2 gate dielectric in (a) and (b) respectively.

4.5 Modified Approach - Dual Gate Mask Process

Being a serial patterning technique, EBL suffers from low throughput processing. Comparing to optical lithography, EBL has to draw the pattern pixel by pixel and this costs a lot of time. In fact, the small feature size is required only for the gate pattern in the gate line definition. However, in previous design, the majority of time is spent on drawing the gate pad, source and drain contact pads (approximately 10^4 μm^2 for each device and costs 40 minutes). It is not effective and only a few devices can be made in one run. Device variation or failure is likely to arise from imperfection of the process, such as the MBE growth substrate. More devices are required for further, stable and conclusive study. Considering that all other processes, such as CVD high-k deposition and implantation, are parallel, EBL becomes the bottle neck of this work. As a result, this section proposes and tests a more effective way of using EBL.

In the modified approach, new optical masks are designed for the gate pad region and contact pads. It is shown in the Appendix 1. Every die has 81 (9 x 9) short channel transistors, a column of test long channel transistors, three TLM patterns, and alignment marks.

In making the TaN gate, there are two steps to define the etch mask for TaN gate electrode and pad. Firstly, the gate line region is drawn by the process. It is the dumbbell shaped region in Fig. 4.10. All gate lines are designed in a way that it will match the spatial distance of the array in the optical mask: the distance is 400 μm in step for both horizontal and vertical directions. Secondly, after Pt lift-off, positive resist is spin-coated onto the wafer. The optical mask, which is made of plastic, is aligned to the gate line by an optical lithography system – mask aligner. When exposure and development are finished, the mask eventually comprises of two parts, the photoresist and Pt hard mask. It is now ready for RIE. Fig. 4.10 shows the top

view of the device after RIE and ashing process. The dumbbell-shape gate line region has a different color to other TaN area because the Pt still remains on TaN. The source and drain contact is made after implantation and RTA activation. It is using the second plastic mask to make the pattern and lift off as labeled in Fig. 4.10. This modified method successfully cuts down the time-consuming serial process and converts it into a parallel one. Over 400 gate patterns for MOSFET can be fabricated in one hour's EBL process. The dramatist increase in efficiency makes the experiment more robust and further detail study possible.

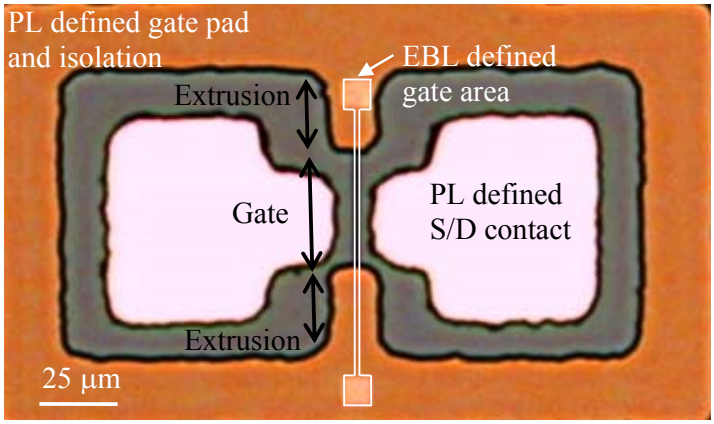


Fig. 4.10 : Short channel InGaAs MOSFET fabricated by the modified dual gate mask approach. The Electron Beam Lithography (EBL) and Photo Lithography (PL) defined areas are shown.

Note that the plastic mask only has a resolution of 30 μm. So it is not possible to make very small pattern or spacing. In the figure, the contact spacing and extrusion of the gate pad is about 20 μm in width. It is made possible by a careful calibration of over exposed photoresist. Besides, the pattern obtained from plastic mask has a rounded corner and non-straight edge. However, this is not a critical issue in our design of process and device.

Note that in Fig. 4.10, the gate width in fact is effectively comprised of two long channel parts and one short channel part. The long channel parts are two extrusions

regions. The mask design has various dimensions for the extrusion ready for use. In the gate width direction, the extrusion has dimensions from 0 to 30 μm. In Fig. 4.10, it is 30 μm. In the gate length direction, the extrusion is 17 μm. It may be observed that the extrusion will contribute an insignificant portion of the drain current depending on its width. This work subtracts this portion of the current from the total current according to the long channel transistor's contribution, and then obtains the normalized short channel transistor drain current. To do this, several long channel transistor of 17 μm gate length is made together in the same mask design.

The MOSFET is fabricated with HfAlO on Type-2 substrate. Both long channel (17 μm) and short channel (600 nm) device are fabricated. It shows extraordinary inversion C-V behavior with small frequency dispersion as illustrated in Fig. 4.11. The I_d-V_g characteristic of the long channel device is demonstrated in Fig. 4.12.

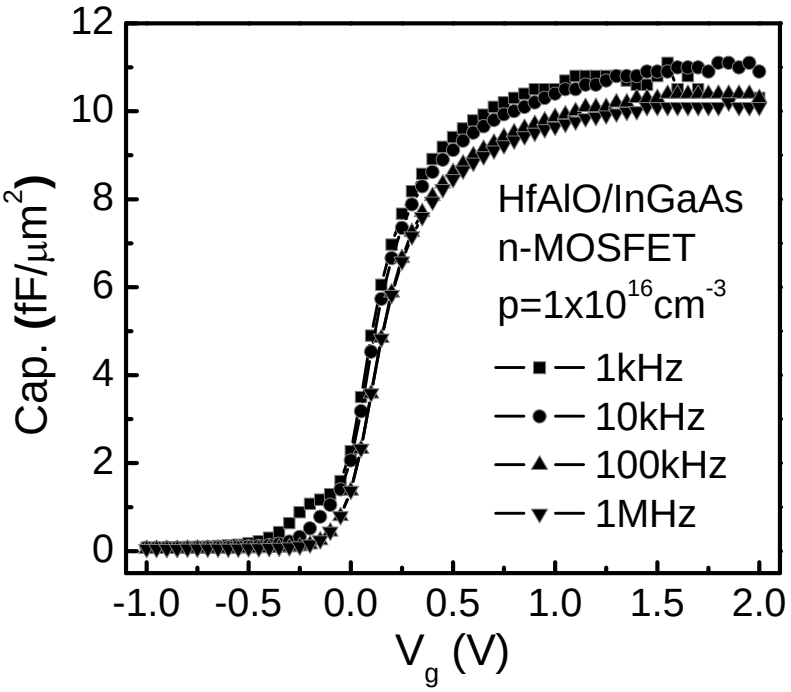


Fig. 4.11 : Inversion C-V characteristic for InGaAs MOSFET with plasma PH_3 passivation for Type-2 substrate.

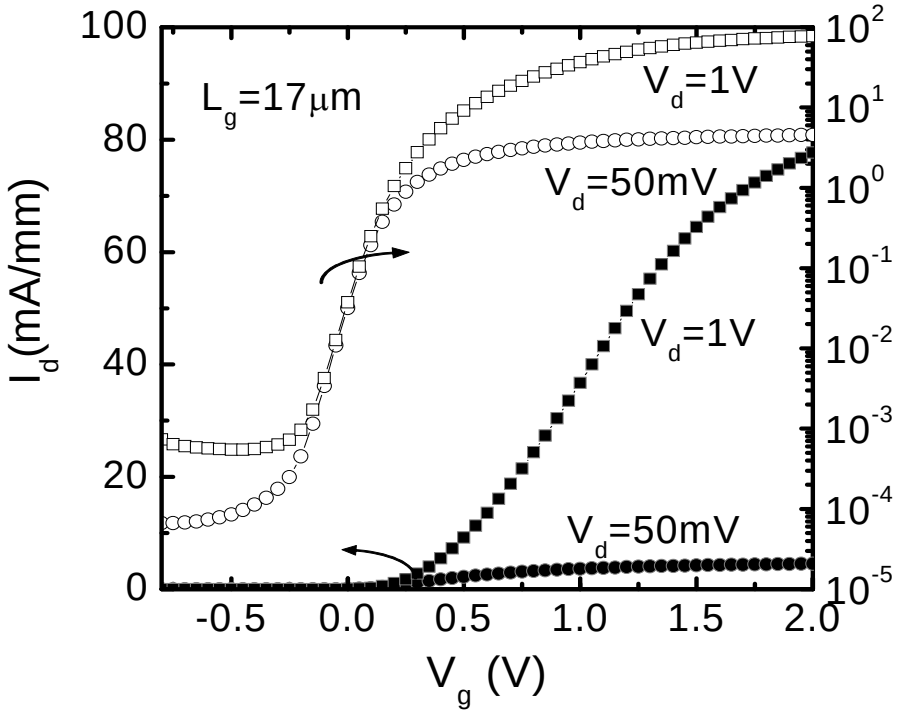


Fig. 4.12 : I_d-V_g characteristic of long channel (17 μm) device is illustrated. The MOSFET is with plasma PH_3 passivation for Type-2 substrate.

So far, short channel devices of 600 nm gate length on Type-2 substrate (refer to Table 1.2 in Chapter 1) are successfully demonstrated with this approach. The device uses the plasma PH_3 passivation described in Chapter 3. The HfAlO has physical thickness of 10 nm. Fig. 4.13 shows the I_d-V_g and G_m-V_g characteristics. The current density is 462 mA/mm at V_g = 2 V and V_d = 1 V. Peak transconductance is 378 mS/mm, without correction. Refer to [4.5], it achieves similar performance with $In_{0.65}Ga_{0.35}As$ substrate with gate length 400 nm and ALD Al_2O_3 under lower biases.

The I_d-V_d characteristics are shown in Fig. 4.14. Gate voltage is from -0.5 V to 3 V in 0.5 V step. The drain bias ranges from 0 to 2 V. Well-behaved output characteristics are observed. It is clearly shows that when V_g > 2 V, the MOSFET current is very close to each other for increasing V_g. The limiting factor for further current/transconductance increase is mainly the series resistance. Maximum current for this device is 851 mA/mm at gate and drain bias of 3 V and 2 V respectively.

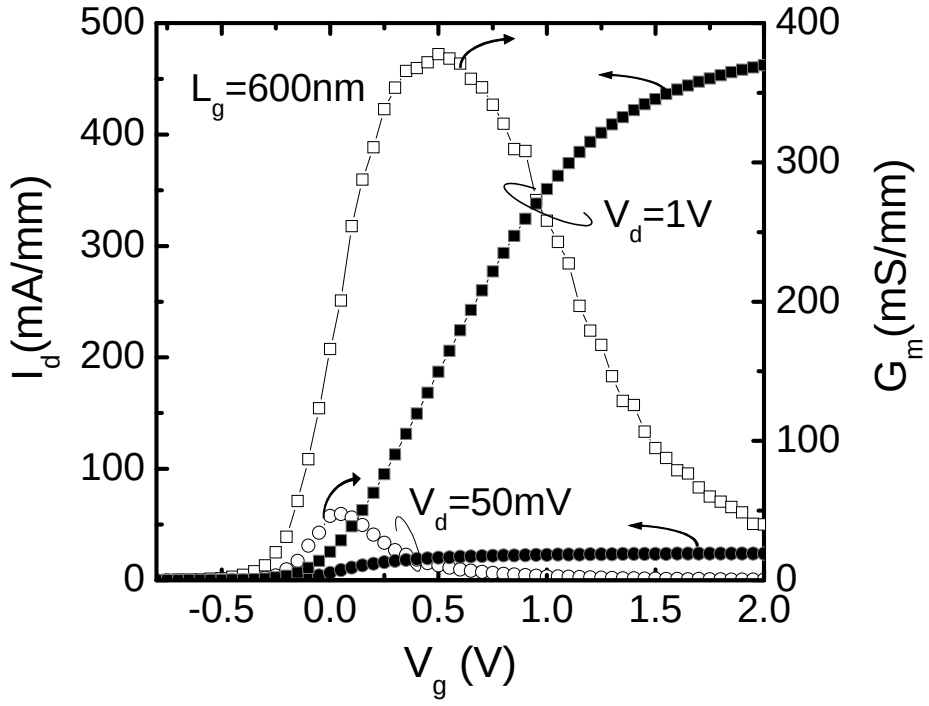


Fig. 4.13 : I_d-V_g and transconductance of 600 nm gate length InGaAs MOSFET on Type-2 substrate with plasma PH_3 passivation.

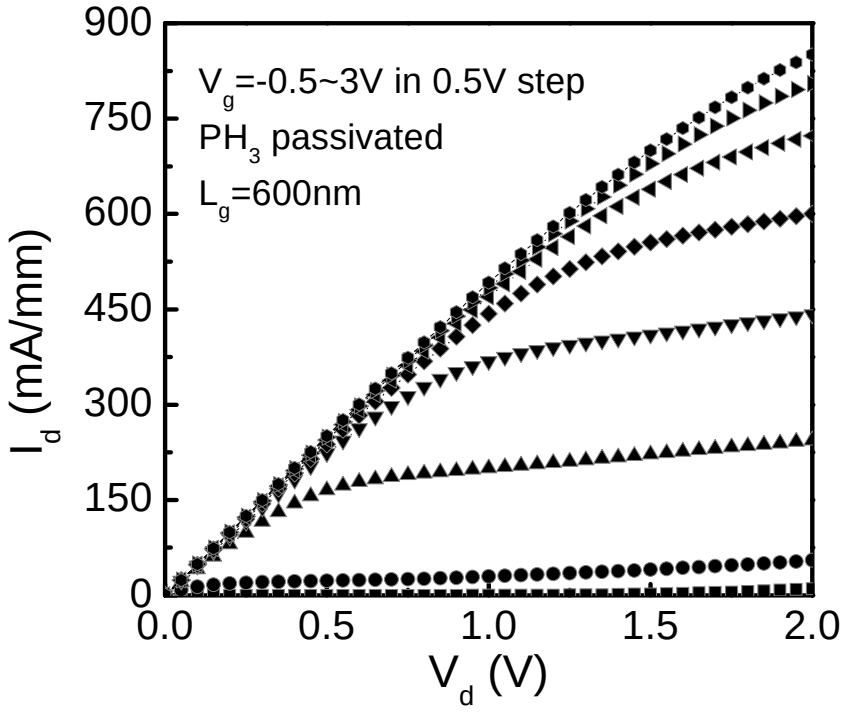


Fig. 4.14 : I_d-V_d of 600 nm gate length InGaAs MOSFET on Type-2 substrate with plasma PH_3 passivation.

4.6 Summary

This chapter discusses the fabrication of nano-sized gate length InGaAs MOSFET. Firstly a new approach is used to define and etch the TaN gate electrode with small feature size. It combined the EBL and hard mask for RIE. Secondly, a suitable inert metal is selected for hard mask. Pt is proven to be a suitable choice of material. Thirdly, using the new approach, a conformal gate line as small as 40 nm is demonstrated. Then, the process integration to make a short channel MOSFET is carried out and the first 95 nm MOSFET without interface passivation is fabricated. In the next step, the drawback of serial time-costly EBL process is identified as the main source of limit for further study. A modified dual mask process is proposed and tested. A successful fabrication of InGaAs MOSFET with gate length of 600 nm and with plasma PH_3 passivation is demonstrated. High performances are reported with a drain current of 851 mA/mm and peak transconductance of 378 mS/mm. Lastly, the limit posed by source and drain series resistance is identified as the main source of technical obstacle to be solved for further device improvement.

4.7 Reference

[4.1]. D.-H. Kim and J.A. del Alamo, "30 nm E-mode InAs PHEMTs for THz and Future Logic Applications," in *IEDM Tech. Dig.*, 2008, pp. 719.

[4.2]. Y. Xuan, Y.Q. Wu, T. Shen, T. Yang, and P.D. Ye "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al_2O_3, HfO_2 and HfAlO as gate dielectrics," in *IEDM Tech. Dig.*, 2007, pp. 637.

[4.3]. K.M. Lee. "Fabrication of Sub-0.5 μm High Electron Mobility Transistors", Ph.D thesis, National University of Singapore, 1998.

[4.4]. M.V. Rao, S.M. Gulwadi, P.E. Thompson, A. Fathimulla and O.A. Aina, "Halogen Lamp Rapid Thermal Annealing of Si- and Be-Implanted $In_{0.53}Ga_{0.47}As$," *J. Elect. Mat*., vol. 18, pp. 131, 1989.

[4.5]. Y. Xuan, Y.Q. Wu and P.D. Ye, "High-Performance Inversion-Type Enhancement-Mode InGaAs MOSFET with Maximum Drain Current Exceeding 1A/mm ," *IEEE Electron Devices Lett.*, vol. 29, no. 4, pp. 294, 2008.

Chapter 5 : Conclusion

The closing chapter of this thesis covers two themes. One is the summary of the work reported in the previous chapter. The other is the recommendation of future research for high mobility channel, especially the InGaAs, MOSFET study.

5.1 Summary of This Work

5.1.1 Modular process and transistor integration

This work started with the MBE growth of InGaAs on InP and GaAs substrate. The control of surface roughness, doping profile and epitaxial thickness are the major concerns. The main starting substrate for device fabrication is InGaAs on InP which has surface doping concentration of $1x10^{17}$ cm^{-3}.

Surface preparation of diluted HF/HCl and $(NH_4)_2S$ to remove the surface native oxide and first layer of passivation are studied. The surface before and after the preparation is compared, showing only a small degradation of surface roughness.

The native oxide formation on GaAs and InGaAs are studied by XPS. After surface cleaning, native oxide on both substrates is removed. When exposed to the ambient environment, Ga- and As- oxide is easier to form on GaAs than InGaAs. Directly deposited HfAlO on GaAs shows evident formation of Ga-oxide and As-oxide, while on InGaAs, these oxides are not detected. MOS capacitor using TaN/HfAlO on GaAs and InGaAs are fabricated. The InGaAs MOS capacitor shows smaller hysteresis. The Valence Band Offset and Conduction Band Offset are studied

by the VB spectra method. Sufficient VBO and CBO are one of the reasons for low gate leakage current.

Implanted Silicon into InGaAs is used to form the n^+ source and drain. It is mainly focusing on two properties, the conductivity of the n^+ region and the rectifying characteristic of the n^+-p junction. Various activation conditions are studied. It is found that 600 ^oC is possible to activate the implanted Silicon and it is promising for low thermal budget source and drain engineering for gate last process.

Integrating all above processes, the MOSFET is fabricated and it demonstrates well-behaved I_d-V_g and I_d-V_d characteristics.

5.1.2 Interface engineering

The interfacial quality of high-k on InGaAs is a concern when studying the MOSFET with directly deposited HfAlO. The subthreshold swing is one measure of the interface trap quality. The subthreshold swing for MOSFET with directly deposited HfAlO is above 200 mV/dec. So the interface is far from satisfaction. A calibrated plasma PH_3 passivation is applied to the InGaAs surface before high-k deposition. It shows improved interface roughness and further reduction of As- oxide formation by a shallow incorporation of P- and N- on the surface.

The MOSFET fabricated by applying plasma PH_3 passivation shows low frequency dispersion and hysteresis in capacitance measurement, indicating low trap concentration at the interface and in the bulk of the dielectric. Transfer and output characteristics show tremendous improvement due to the passivation effect. Four times increase in drain current and a record value of 96 mV/dec in subthreshold swing are reported. The channel mobility of electron is 1600 $cm^2/V.s$ as measured by the

split C-V method without correction method considering interface trap and parasitic resistances.

5.1.3 Short channel MOSFET

The short channel MOSFET is enabled by the self-alignment fabrication process. A new method is proposed to fabricate the small gate line device. In the first phase, the EBL test process and selection of hard mask material are carried out. Pt is selected as material for hard mask. Conformal pattern with line width of 40 nm is successfully demonstrated. In the second phase, the InGaAs MOSFET of small gate length is fabricated by this method. It uses directly deposited HfO_2 as gate dielectric, and has a gate length of 95 nm. Well-behaved transistor characteristics are shown. In the third phase of the short channel development, a modified approach is proposed to convert part of the costly serial EBL process to parallel photolithography process. It improves fabrication yield dramatically. And the 600 nm gate length MOSFET with plasma PH_3 passivation is made. It demonstrates drain current above 851 mA/mm at bias of $V_d = 2$ V, $V_g = 3$ V.and peak transconductance 378 mS/mm.

5.1.4 Summary

As mentioned in Chapter 1, the objective of this work is to fabricate a novel InGaAs MOSFET and analyze its performance with the figure of merit for logic devices. A novel fabrication flow is proposed and carried out, which emphasizes on the CMOS compatible material and process, such as the top down RIE pattern of gate electrode, self-aligned source and drain fabrication.

This work has studied several fundamental problems in the way of developing III-V high mobility MOSFET. From the process integration, to interface engineering to device scaling, the results yield insights into III-V's application for sub 32 nm CMOS. It forms the basic reference of further exploration of the III-V's promise as candidates for CMOS logic circuit device, and the solid fundamental for future research to compare III-V MOSFET performance with the Silicon or Strained-Silicon CMOS.

5.2 Future Work

5.2.1 Advanced interface engineering

This work has shown that significant performance leap is achieved by plasma PH_3 passivation. However, there is still room for improvement for better interfacial quality. Though a recorded subthreshold swing is reported in Chapter 3 of 96 mV/dec, this value is still unsatisfactory comparing with the fundamental physical limit of 60 mV/dec at room temperature. Even benchmarked with state-of-art Silicon CMOS and some of the InGaAs HEMTs, this value is still high. On the other hand, C-V characteristic and hysteresis are not as good as what is reported in Silicon as well. For future threshold voltage requirement of around 0.1 V, the hysteresis of a few tens of milli-volts is undesirable. It is expected that better interface between InGaAs and high-k dielectric can improve the performance.

5.2.2 Reduction in parasitic elements

Discussed in both Chapter 3 and 4, the parasitic resistances become the major limiting factor for achieving higher drain current and transconductance. It prohibits

the analysis of intrinsic characteristic of InGaAs MOSFET. There are correction methods to extract the intrinsic electric data from extrinsic measurement results such as interface trap correction and series resistance correction. However, it is favorable to obtain the analysis from direct measurement mainly because of two reasons. Firstly, those correction methods initially developed for Silicon involve assumptions and data processing that might not be suitable or accurate for the present III-V MOSFET. Some improper assumption and handling of data may result in large discrepancy. Secondly, the ultimate device that is fabricated on the IC chip, should be the one with well-engineered parasitic. It is of great significance to study and reduce the parasitic elements. One approach is to increase the activation efficiency and bring the source and drain contact closer to the channel. The development of III-V metallization and spacer technology are practical solutions.

5.2.3 Novel device structures

As approaching smaller gate length, the control of short channel effect becomes increasingly important. It is expected that future generation of MOSFET would not be limited to planer bulk structure. In Silicon technology, the thin body or ultra thin body structure has been well developed and ready for use in next generation according to ITRS. Three dimensional devices are on the way of development. These include double gate, Fin-FET and Gate-All-Around (GAA) FET. Recent strained Silicon nanowire FET has achieved 5 nm in gate length (Liow *VLSI* 2008). If III-V were to be used for future CMOS devices, it is highly likely that such 3D structure is required.

The Silicon CMOS can achieve its present small feature size, an important platform is the self-alignment process. Self-alignment is a key step for the development of MOSFET with very small gate line feature in VLSI circuit. For the

first time, this work has developed the self-aligned fabrication method of InGaAs MOSFET and indicates a highly-scalable III-V MOSFET technology. It should be able to serve as the key for ultra short channel 3D III-V MOSFET development.

Appendix 1 : Mask Catalog

The plastic mask (**JEROME NOV08**) is designed using AutoCAD. It is divided into 25 regions. It includes the **GATE** mask (yellow), **CONTACT** mask (blue), **TLM** mask (red), **MESA** mask (green) and **SPARE** mask (grey).

The effective drawing window size of one plastic mask is 11x11 cm^2. And the 25 regions are set in the drawing window as shown in Fig. A.1. Every region has a size of 2x2 cm^2. The respective patterns in the mask are shown below. All masks contain pattern for both positive and negative photoresist exposures.

- **GATE** mask Color code – yellow. Label – A:1-5, B:1, and C:3-4.
- **CONTACT** mask Color code – blue. Label – B:2-5, C:1-2, and C:5.
- **TLM** mask Color code – red. Label – E:1-2.
- **MESA** mask Color code – green. Label – D:1-5.
- **SPARE** mask Color code – grey. Label – E:3-5.

Label are denoted as "Column:Row".

The typical chip size for EBL-made transistor is about 1x1 cm^2. So the individual **GATE** mask and **CONTACT** mask are made according to this size. The layout is shown in Fig. A.1 (a) and (b) for **GATE** and **CONTACT** respectively. **GATE** masks in different region contain different gate width pattern, from 30 to 90 μm. **CONTACT** mask contains minimum contact pattern spacing of 30 μm and width from 30 to 60 μm. **GATE** mask and **CONTACT** mask can be selected to align with each other. Every device occupies an area of 400x400 μm^2.

The TLM pattern is shown in Fig. A.2. (a) is the isolation pattern. (b) is the contact pattern. Those two masks are aligned with each other.

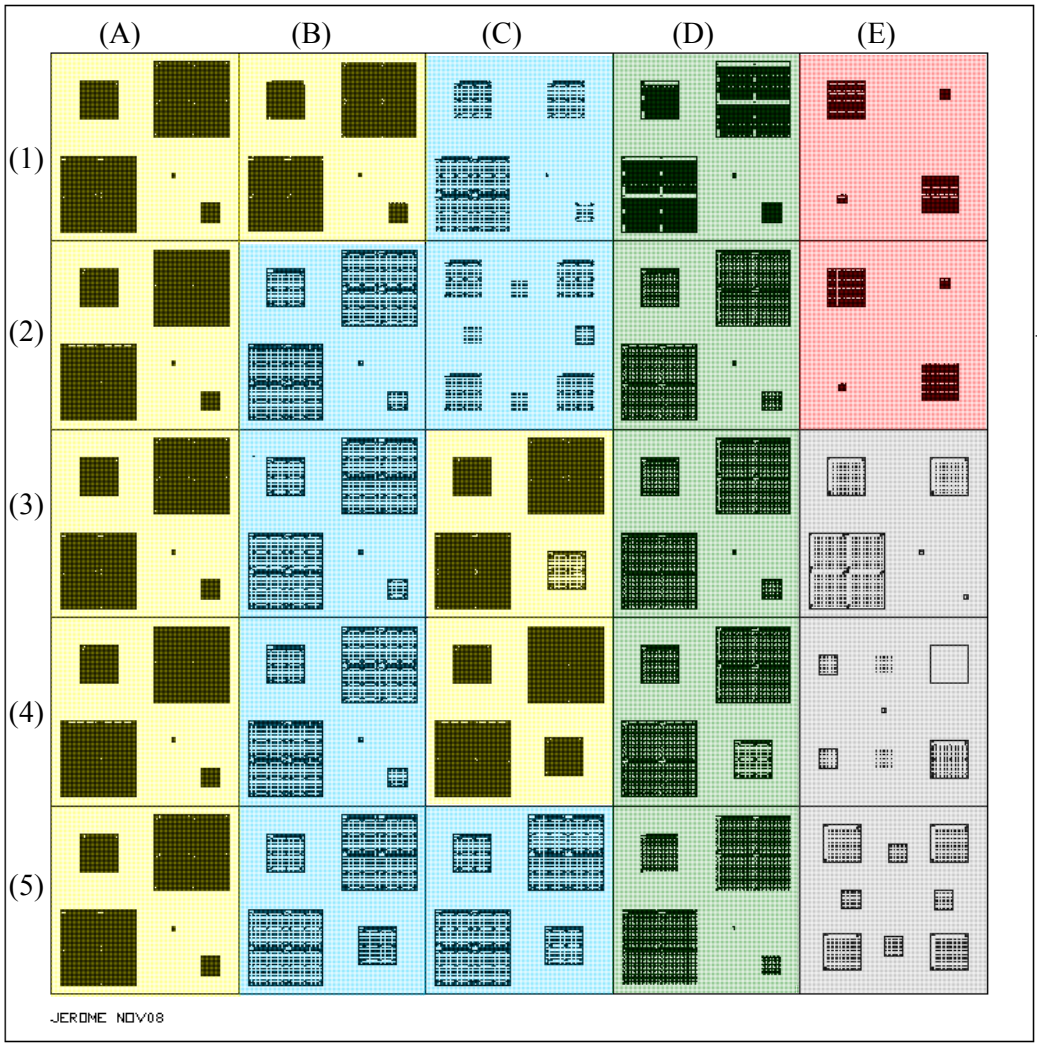
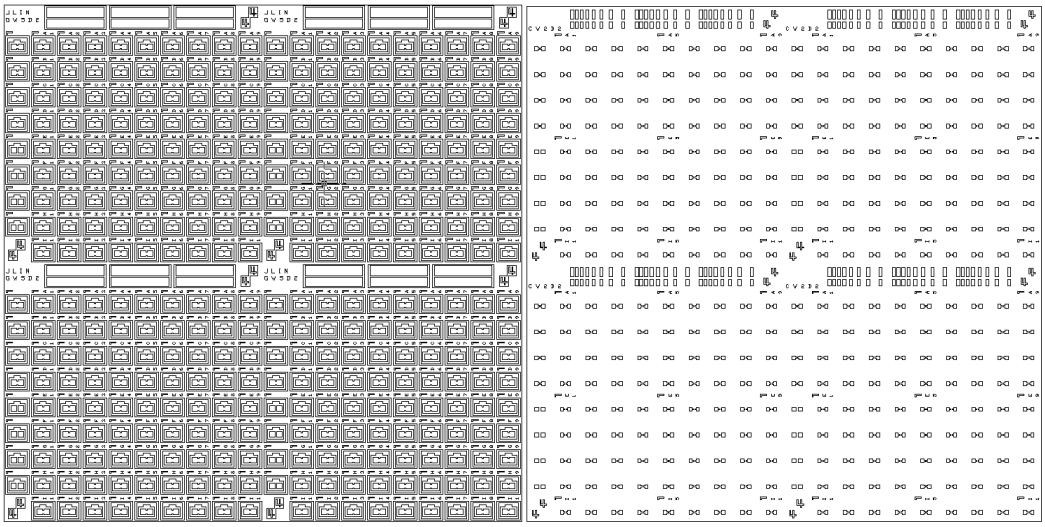
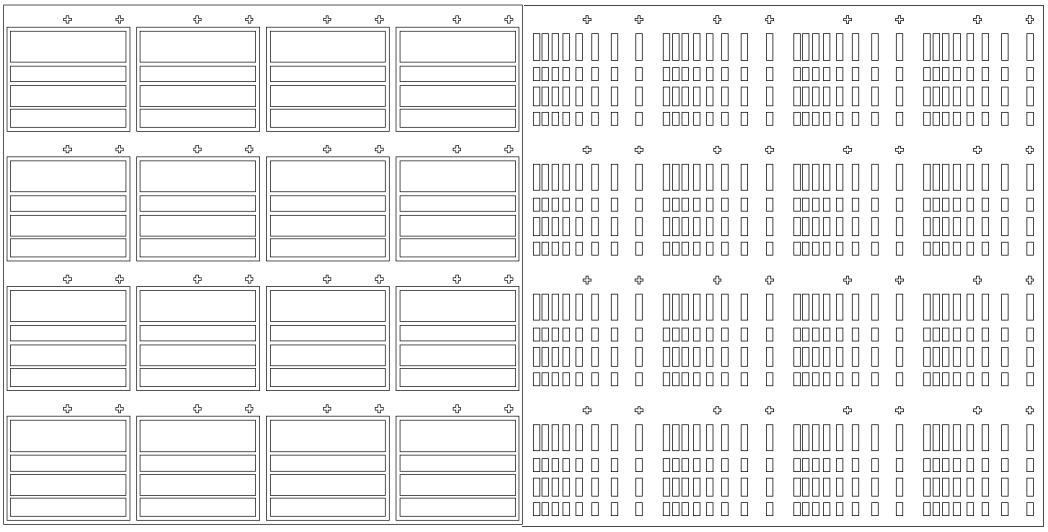


Fig. A.1 : Layout for plastic mask "JEROME NOV08". Five regions are denoted in different color and serve different function. Including the **GATE** mask (yellow), **CONTACT** mask (blue), **TLM** mask (red), **MESA** mask (green) and **SPARE** mask (grey).



(a) (b)

Fig. A.2 : (a) 4-die gate mask and (b) 4-die contact mask pattern.



(a) (b)

Fig. A.3 : (a) TLM isolation and (b) TLM contact pattern.

Appendix 2 : List of Publications

- Publications related to works reported in this thesis

Journal and letter

[1]. J. Q. Lin, H. J. Oh, S. A. B. Suleiman, G. Q. Lo, and D. Z. Chi, and S. J. Lee, "Sub-micron InGaAs Metal-Oxide-Semiconductor Field Effect Transistor with Plasma PH_3 Passivation and Substrate Dependency Study", submitted for publication.

[2]. J. Lin, H.-J. Oh, W. Yang, G.-Q. Lo, and S.J. Lee, "Performance Improvement of Inversion-Mode $In_{0.53}Ga_{0.47}As$ n-MOSFET by Plasma PH_3 Passivation for High-k Integration on $In_{0.53}Ga_{0.47}As$ Substrate," submitted for publication.

[3]. H. J. Oh, J. Lin, and S.J. Lee, "Origin of Enhanced Performance in plasma PH_3-passivated InGaAs NMOSFET fabricated with Self-aligned Process and MOCVD High-k/Metal Gate Structure," submitted for publication.

[4]. J. Lin, S.J. Lee, H.J. Oh, G.Q. Lo, D.L. Kwong, and D.Z. Chi, "Inversion-mode Self-aligned $In_{0.53}Ga_{0.47}As$ N-Channel Metal-Oxide-Semiconductor Field-Effect-Transistor with HfAlO Gate Dielectric and TaN Metal Gate," *IEEE Electron Devices Lett.*, vol. 29, no. 9, pp. 977, 2008.

[5]. H.J. Oh, J. Lin, S.J. Lee, G.K. Dalapati, A. Sridhara, D.Z. Chi, S.J. Chua, G.Q. Lo, and D.L. Kwong, "Study on interfacial properties of InGaAs and GaAs integrated with chemical-vapor-deposited high-k gate dielectrics using X-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol.93, pp. 062107, 2008.

Conference

[6]. J. Lin, S.J. Lee, H.J. Oh, W. Yang, G.Q. Lo, D.L. Kwong and D.Z. Chi, "Plasma PH_3-Passivated High Mobility Inversion InGaAs MOSFET Fabricated with Self-Aligned Gate First Process and HfO_2/TaN Gate Stack", in *IEDM* Tech. Dig., 2008, pp. 401-404. (IEEE Roger A. Haken Award 2008)

[7]. J. Lin, S.J. Lee, H.J. Oh, G.K. Dalapati, D.Z. Chi, G.Q. Lo, and D.L. Kwong, "Enhancement-Mode $In_{0.53}Ga_{0.47}As$ n-MOSFET with Self-aligned Gate-first Process and CVD HfAlO Gate Dielectric" in *SSDM* Tech. Dig., 2008, pp. 30-31.

[8]. H. J. Oh, J. Q. Lin, S. A. B. Suleiman, G. Q. Lo, D. L. Kwong, D. Z. Chi, and S. J. Lee, "Thermally Robust Phosphorous Nitride Interface Passivation for InGaAs Self-Aligned Gate-First n-MOSFET Integrated with High-k Dielectric", in *IEDM* Tech. Dig., 2009, pp. 339-342.

- Other publications

[9]. C. Shen, J. Lin, E.-H. Toh, K.-F. Chang, P. Bai, C.-H. Heng, G. S. Samudra, and Y.-C. Yeo, "On the performance limit of impact-ionization transistors," in *IEDM* Tech. Dig., 2007, pp. 117-120.

[10]. C. Shen, E.-H. Toh, J. Lin, C.-H. Heng, D. Sylvester, G. Samudra, and Y.-C. Yeo, "A Physics-based Compact Model for I-MOS Transistors," in *SSDM* Tech. Dig., 2007, pp. 608-609.

[11]. K.-W. Ang, J. Lin, C.-H. Tung, N. Balasubramanian, G. Samudra, and Y.-C. Yeo, "Beneath-The- Channel Strain-Transfer-Structure (STS) and Embedded Source/Drain Stressors for Strain and Performance Enhancement of Nanoscale MOSFETs," *Symp. on VLSI Tech.*, 2007, pp. 42-43.

[12]. Y.-C. Yeo, K.-W. Ang, J. Lin, C.-S. Lam, "Strain-transfer structure beneath the transistor channel for increasing the strain effects of lattice-mismatched source and drain stressor," in MRS Spring, 2007.

[13]. J. Lin, E.-H. Toh, C. Shen, D. Sylvester, C.-H. Heng, G. Samudra, and Y.-C. Yeo, "Compact HSPICE model for IMOS device," *Electronics Lett.*, vol. 44, issue 2, pp. 91-92, 2008.

[14]. K.-W. Ang, J. Lin, C.-H. Tung, N. Balasubramanian, G. S. Samudra, and Y.-C. Yeo, "Strained n-MOSFET with embedded source/drain stressors and strain-transfer structure (STS) for enhanced transistor performance," *IEEE Trans. Electron Devices*, vol. 55, no. 3, 2008. (IEEE Paul Rappaport Award 2008)

Appendix 3 : List of Awards

- IEEE Electron Device Society Masters Student Fellowship 2008,
- IEEE Roger A. Haken Award 2008,

  The best student paper in the *International Electron Device Meeting*, 2008

- IEEE Paul Rappaport Award 2008 (Co-Recipient),

  The best paper published in the *IEEE Transactions on Electron Devices*, 2008